PMDT290UNE

20 V, 800 mA dual N-channel Trench MOSFET

Rev. 1 — 13 September 2011　　　　　　　　　　　**Product data sheet**

1. Product profile

1.1 General description

Dual N-channel enhancement mode Field-Effect Transistor (FET) in an ultra small and flat lead SOT666 Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

1.2 Features and benefits

- Very fast switching
- Trench MOSFET technology
- ESD protection up to 2 kV
- AEC-Q101 qualified

1.3 Applications

- Relay driver
- High-speed line driver
- Low-side loadswitch
- Switching circuits

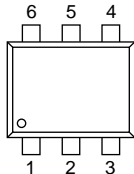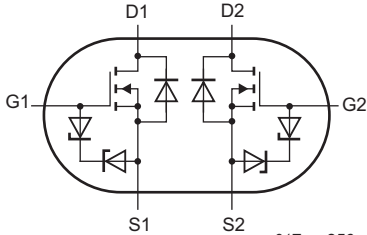### 1.4 Quick reference data

Table 1.　Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
V_{DS}	drain-source voltage	T_j = 25 °C		-	-	20	V
V_{GS}	gate-source voltage			-8	-	8	V
I_D	drain current	V_{GS} = 4.5 V; T_{amb} = 25 °C	[1]	-	-	800	mA
Static characteristics (per transistor)							
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 500 mA; T_j = 25 °C		-	290	380	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm^2.

2. Pinning information

Table 2.   Pinning information

Pin	Symbol	Description
1	S1	source TR1
2	G1	gate TR1
3	D2	drain TR2
4	S2	source TR2
5	G2	gate TR2
6	D1	drain TR1

Simplified outline

SOT666

Graphic symbol

017aaa256

3. Ordering information

Table 3.   Ordering information

Type number	Package		
	Name	**Description**	**Version**
PMDT290UNE	-	plastic surface-mounted package; 6 leads	SOT666

4. Marking

Table 4.   Marking codes

Type number	Marking code
PMDT290UNE	AE

5. Limiting values

Table 5.   Limiting values

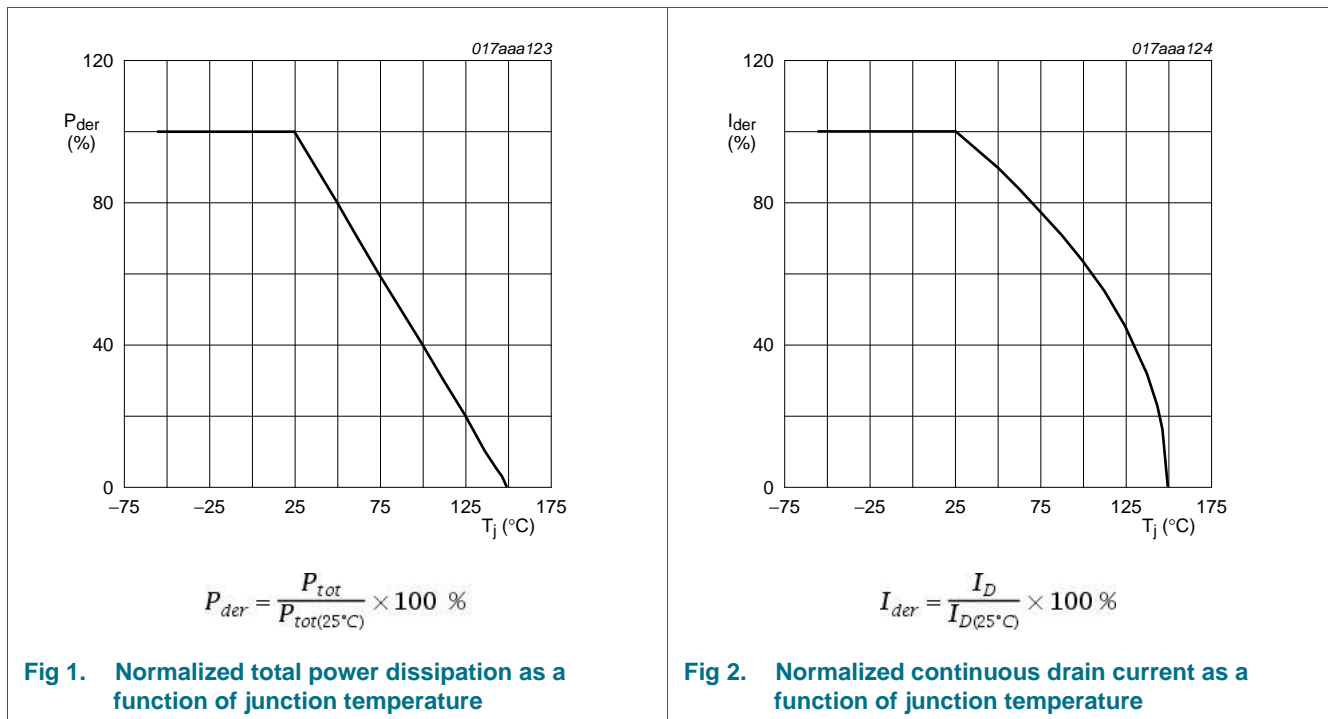*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V_{DS}	drain-source voltage	T_j = 25 °C		-	20	V
V_{GS}	gate-source voltage			-8	8	V
I_D	drain current	V_{GS} = 4.5 V; T_{amb} = 25 °C	[1]	-	800	mA
		V_{GS} = 4.5 V; T_{amb} = 100 °C	[1]	-	500	mA
I_{DM}	peak drain current	T_{amb} = 25 °C; single pulse; t_p ≤ 10 µs		-	3.2	A
P_{tot}	total power dissipation	T_{amb} = 25 °C	[2]	-	330	mW
			[1]	-	390	mW
		T_{sp} = 25 °C		-	1090	mW
Per device						
P_{tot}	total power dissipation	T_{amb} = 25 °C	[2]	-	500	mW
T_j	junction temperature			-55	150	°C
T_{amb}	ambient temperature			-55	150	°C

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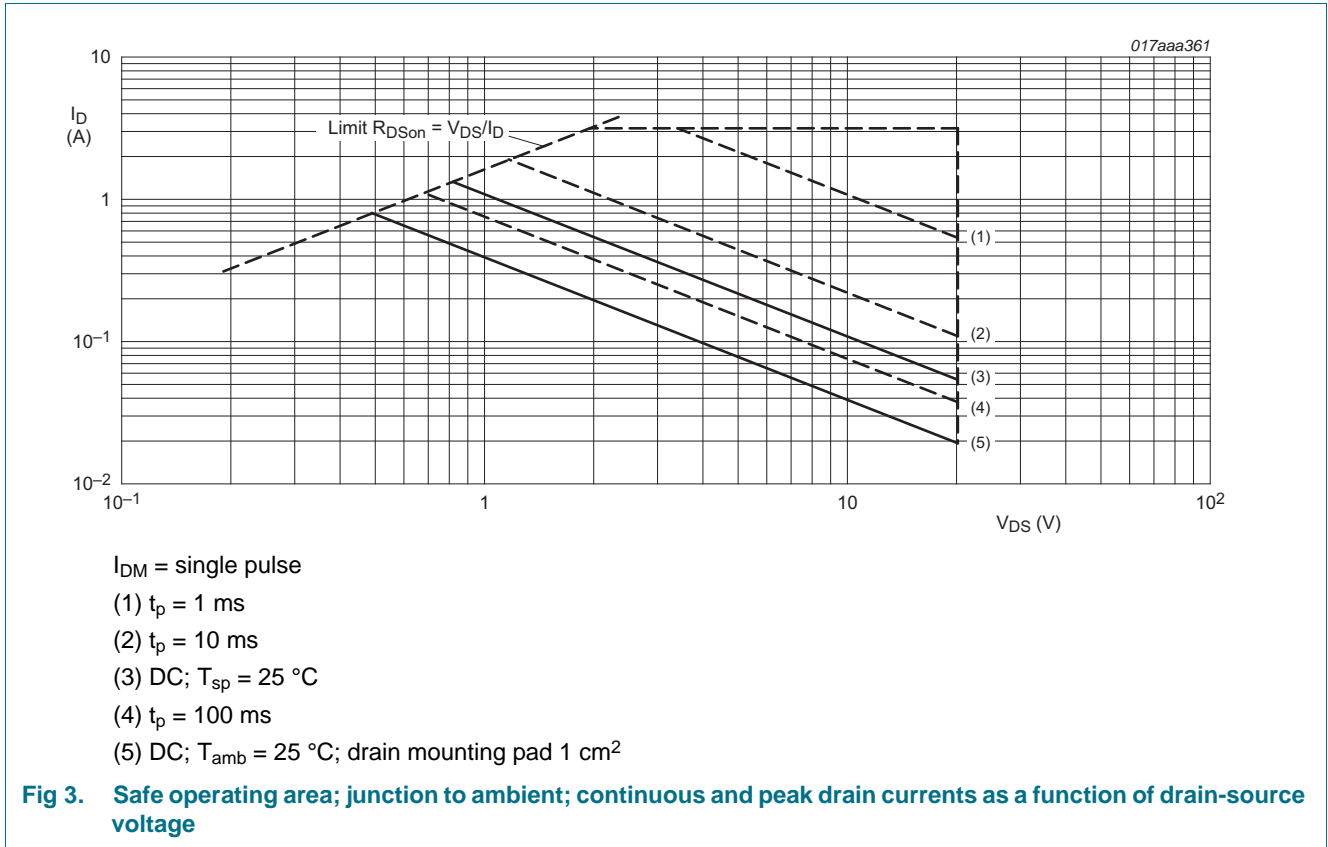**Rev. 1 — 13 September 2011**

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Table 5. **Limiting values** *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
T_{stg}	storage temperature			-65	150	°C
Source-drain diode						
I_S	source current	T_{amb} = 25 °C		-	370	mA
ESD maximum rating						
V_{ESD}	electrostatic discharge voltage	HBM	[3]	-	2000	V

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm2.

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[3] Measured between all pins.

$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100 \ \%$$

Fig 1. **Normalized total power dissipation as a function of junction temperature**

$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100 \ \%$$

Fig 2. **Normalized continuous drain current as a function of junction temperature**

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I_{DM} = single pulse

(1) t_p = 1 ms

(2) t_p = 10 ms

(3) DC; T_{sp} = 25 °C

(4) t_p = 100 ms

(5) DC; T_{amb} = 25 °C; drain mounting pad 1 cm²

Fig 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	330	380	K/W
			[2]	-	280	320	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	-	115	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	250	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm².

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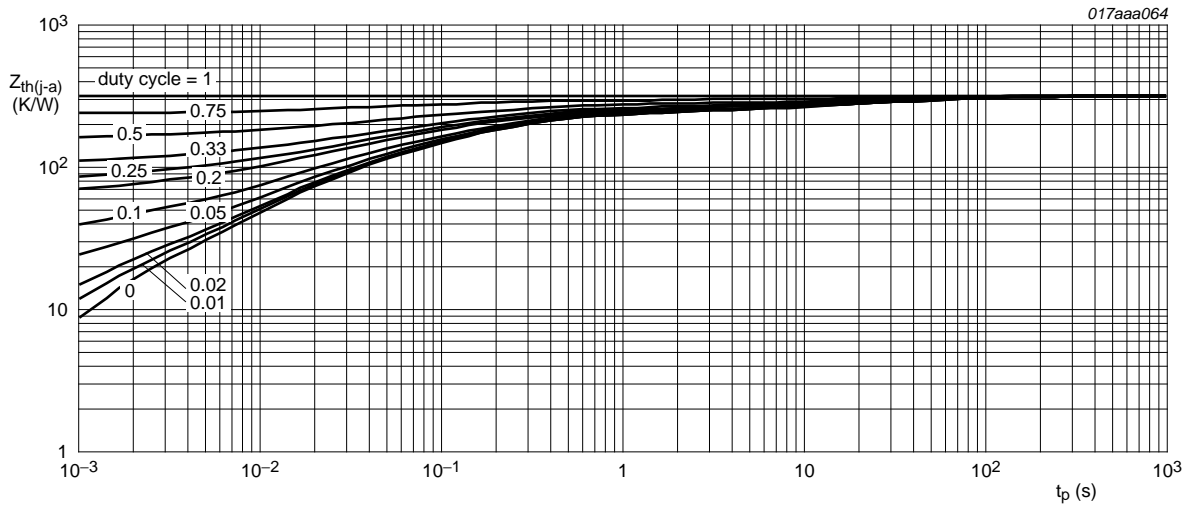
FR4 PCB; standard footprint

Fig 4. **Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**

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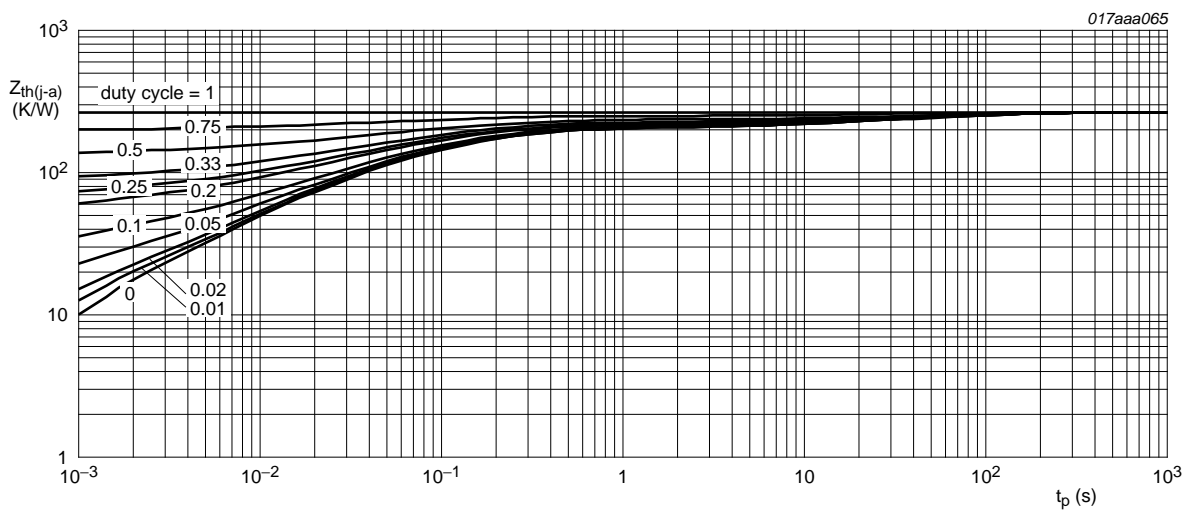
FR4 PCB, mounting pad for drain 1 cm^2

Fig 5. **Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**

7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics (per transistor)						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	20	-	-	V
V_{GSth}	gate-source threshold voltage	I_D = 250 µA; V_{DS} = V_{GS}; T_j = 25 °C	0.5	0.75	0.95	V
I_{DSS}	drain leakage current	V_{DS} = 20 V; V_{GS} = 0 V; T_j = 25 °C	-	-	1	µA
		V_{DS} = 20 V; V_{GS} = 0 V; T_j = 150 °C	-	-	10	µA
I_{GSS}	gate leakage current	V_{GS} = 8 V; V_{DS} = 0 V; T_j = 25 °C	-	-	2	µA
		V_{GS} = -8 V; V_{DS} = 0 V; T_j = 25 °C	-	-	2	µA
		V_{GS} = 4.5 V; V_{DS} = 0 V; T_j = 25 °C	-	-	500	nA
		V_{GS} = -4.5 V; V_{DS} = 0 V; T_j = 25 °C	-	-	500	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 500 mA; T_j = 25 °C	-	290	380	mΩ
		V_{GS} = 4.5 V; I_D = 500 mA; T_j = 150 °C	-	460	610	mΩ
		V_{GS} = 2.5 V; I_D = 400 mA; T_j = 25 °C	-	420	620	mΩ
		V_{GS} = 1.8 V; I_D = 100 mA; T_j = 25 °C	-	600	1100	mΩ
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 200 mA; T_j = 25 °C	-	1.6	-	S
Dynamic characteristics (per transistor)						
$Q_{G(tot)}$	total gate charge	V_{DS} = 10 V; I_D = 500 mA; V_{GS} = 4.5 V; T_j = 25 °C	-	0.45	0.68	nC
Q_{GS}	gate-source charge		-	0.15	-	nC
Q_{GD}	gate-drain charge		-	0.15	-	nC
C_{iss}	input capacitance	V_{DS} = 10 V; f = 1 MHz; V_{GS} = 0 V; T_j = 25 °C	-	55	83	pF
C_{oss}	output capacitance		-	15	-	pF
C_{rss}	reverse transfer capacitance		-	7	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 10 V; R_L = 250 Ω; V_{GS} = 4.5 V; $R_{G(ext)}$ = 6 Ω; T_j = 25 °C	-	6	12	ns
t_r	rise time		-	4	-	ns
$t_{d(off)}$	turn-off delay time		-	86	172	ns
t_f	fall time		-	31	-	ns
Source-drain diode (per transistor)						
V_{SD}	source-drain voltage	I_S = 300 mA; V_{GS} = 0 V; T_j = 25 °C	0.48	0.77	1.2	V

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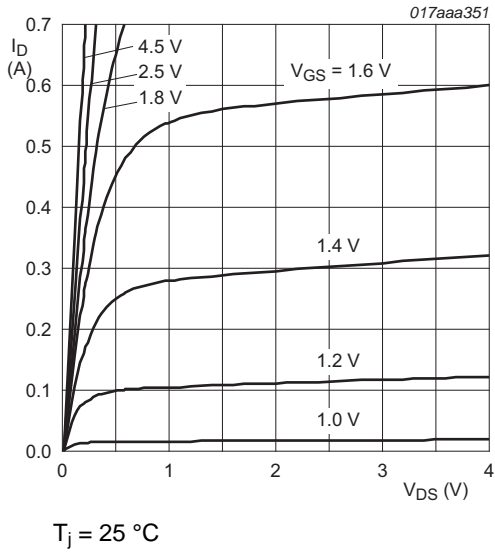
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017aaa351

$T_j = 25\ °C$

Fig 6. **Output characteristics: drain current as a function of drain-source voltage; typical values**

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$T_j = 25\ °C;\ V_{DS} = 5\ V$

(1) minimum values

(2) typical values
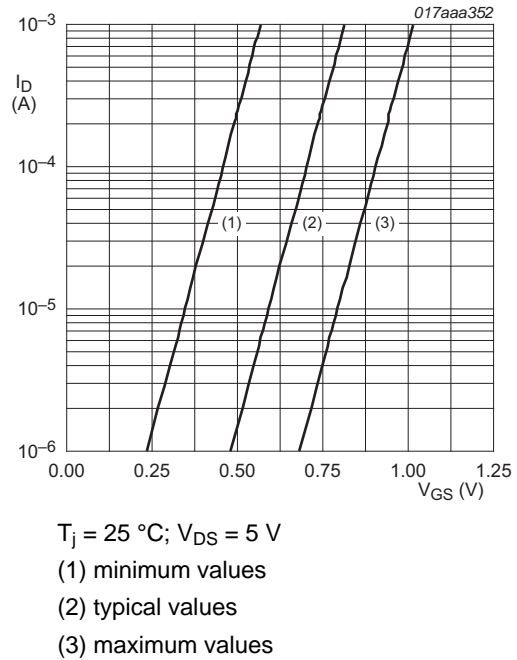
(3) maximum values

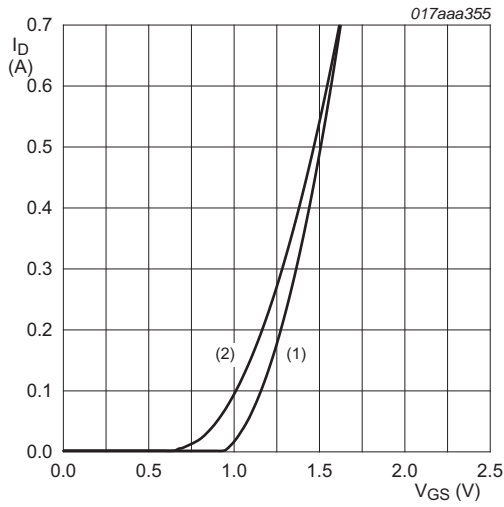**Fig 7.** **Sub-threshold drain current as a function of gate-source voltage**

017aaa353
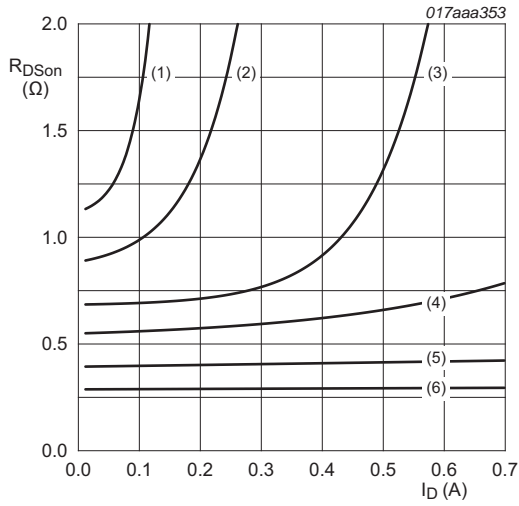
$T_j = 25\ °C$

(1) $V_{GS} = 1.3\ V$

(2) $V_{GS} = 1.4\ V$

(3) $V_{GS} = 1.6\ V$

(4) $V_{GS} = 1.8\ V$

(5) $V_{GS} = 2.5\ V$

(6) $V_{GS} = 4.5\ V$

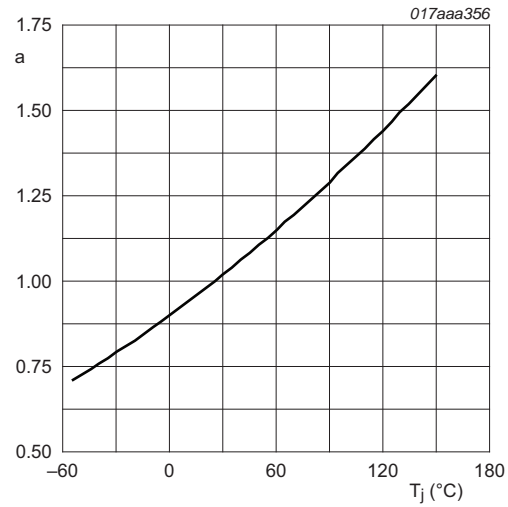**Fig 8.** **Drain-source on-state resistance as a function of drain current; typical values**

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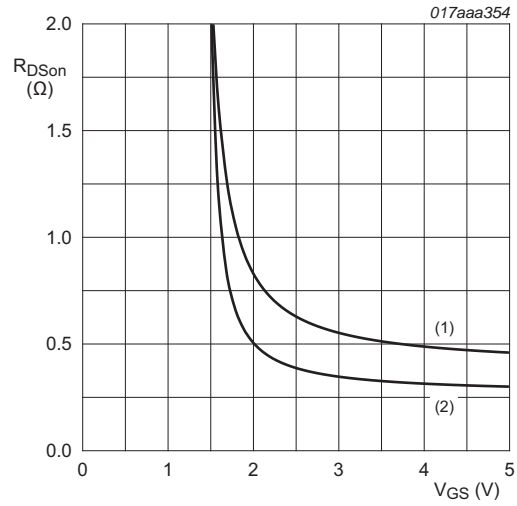
$I_D = 400\ mA$

(1) $T_j = 150\ °C$

(2) $T_j = 25\ °C$

Fig 9. **Drain-source on-state resistance as a function of gate-source voltage; typical values**

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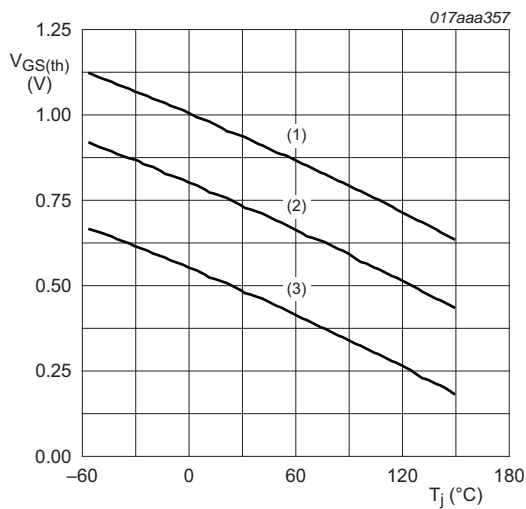
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$V_{DS} > I_D \times R_{DSon}$

(1) $T_j = 25\ °C$

(2) $T_j = 150\ °C$

**Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values**

$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

**Fig 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values**

$I_D = 0.25\ mA;\ V_{DS} = V_{GS}$

(1) maximum values

(2) typical values

(3) minimum values

Fig 12. Gate-source threshold voltage as a function of junction temperature
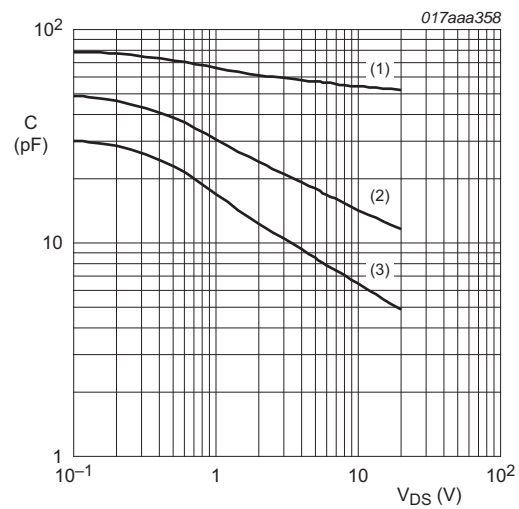
$f = 1\ MHz;\ V_{GS} = 0\ V$

(1) C_{iss}

(2) C_{oss}

(3) C_{rss}

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

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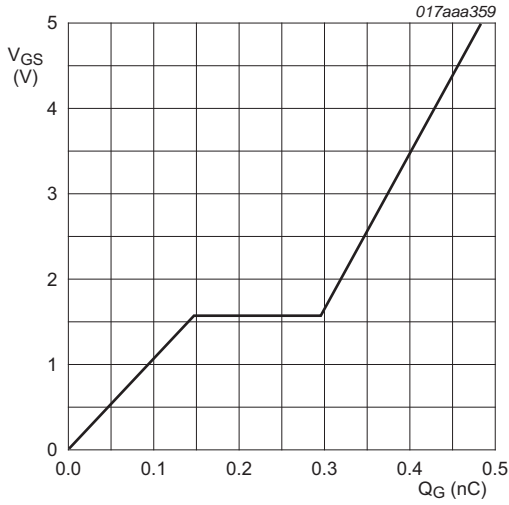
$I_D = 0.5$ A; $V_{DS} = 10$ V; $T_{amb} = 25$ °C

Fig 14. Gate-source voltage as a function of gate charge; typical values
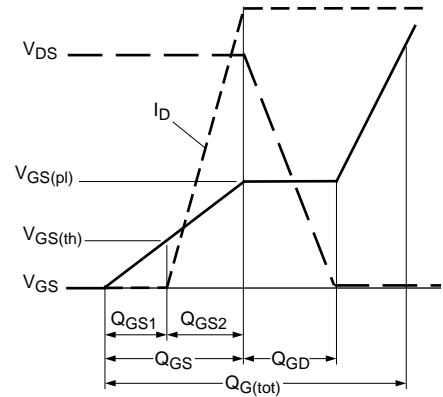
Fig 15. Gate charge waveform definitions
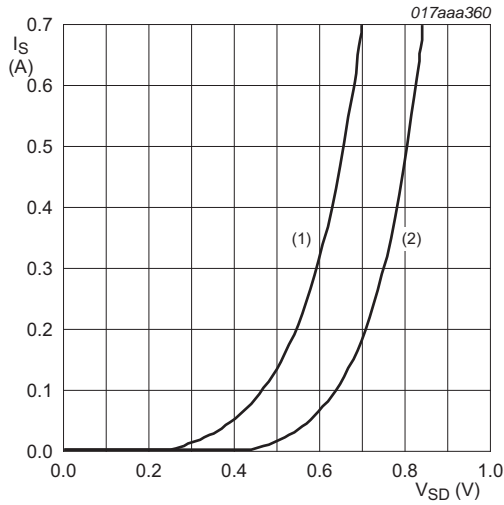
$V_{GS} = 0$ V
(1) $T_j = 150$ °C
(2) $T_j = 25$ °C

Fig 16. Source current as a function of source-drain voltage; typical values

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8. Test information

duty cycle $\delta = \dfrac{t_1}{t_2}$

006aaa812

Fig 17. Duty cycle definition

8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

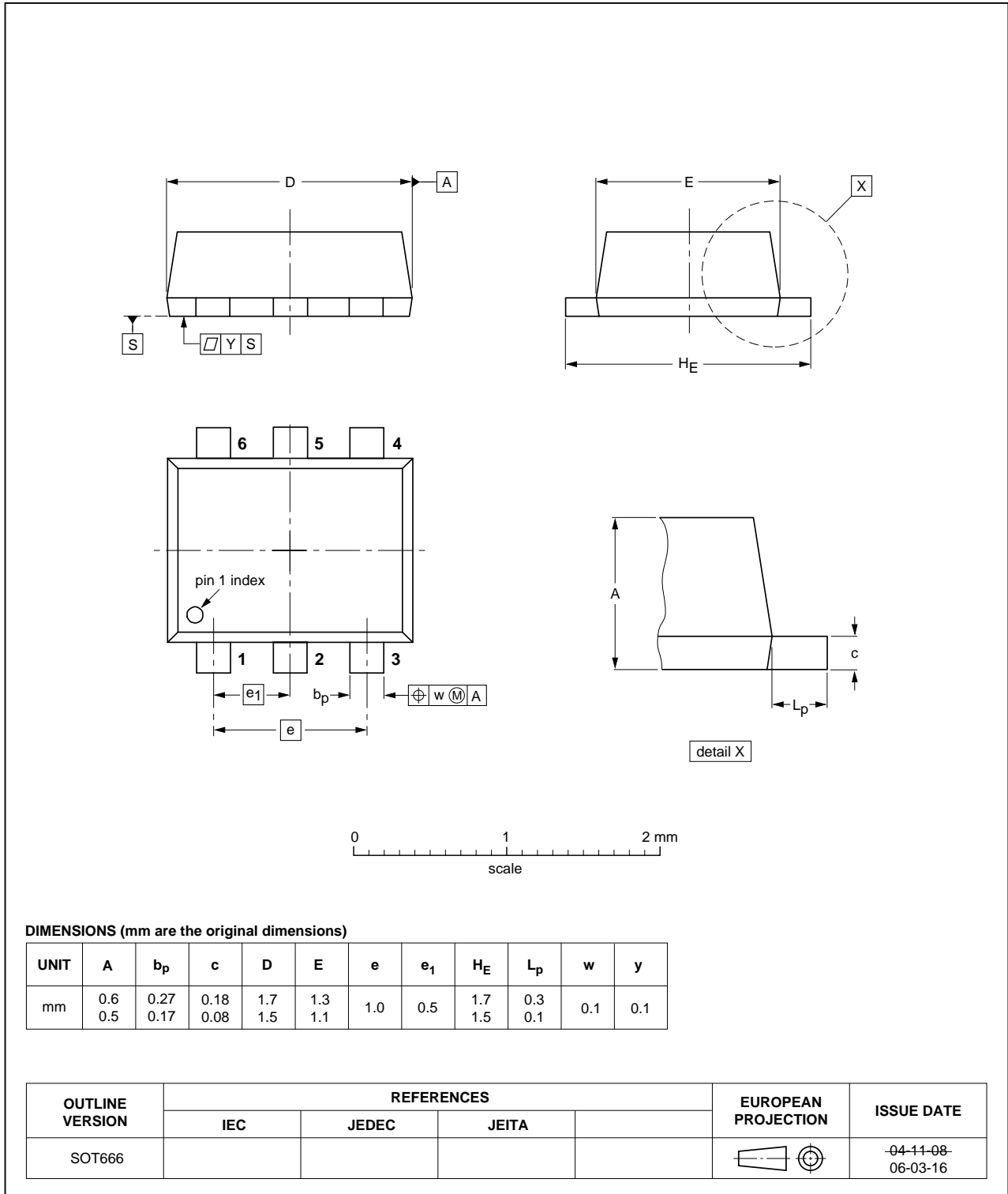## 9. Package outline

Plastic surface-mounted package; 6 leads

SOT666

DIMENSIONS (mm are the original dimensions)

UNIT	A	b_p	c	D	E	e	e_1	H_E	L_p	w	y
mm	0.6 0.5	0.27 0.17	0.18 0.08	1.7 1.5	1.3 1.1	1.0	0.5	1.7 1.5	0.3 0.1	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT666						~~04-11-08~~ 06-03-16

Fig 18. Package outline SOT666
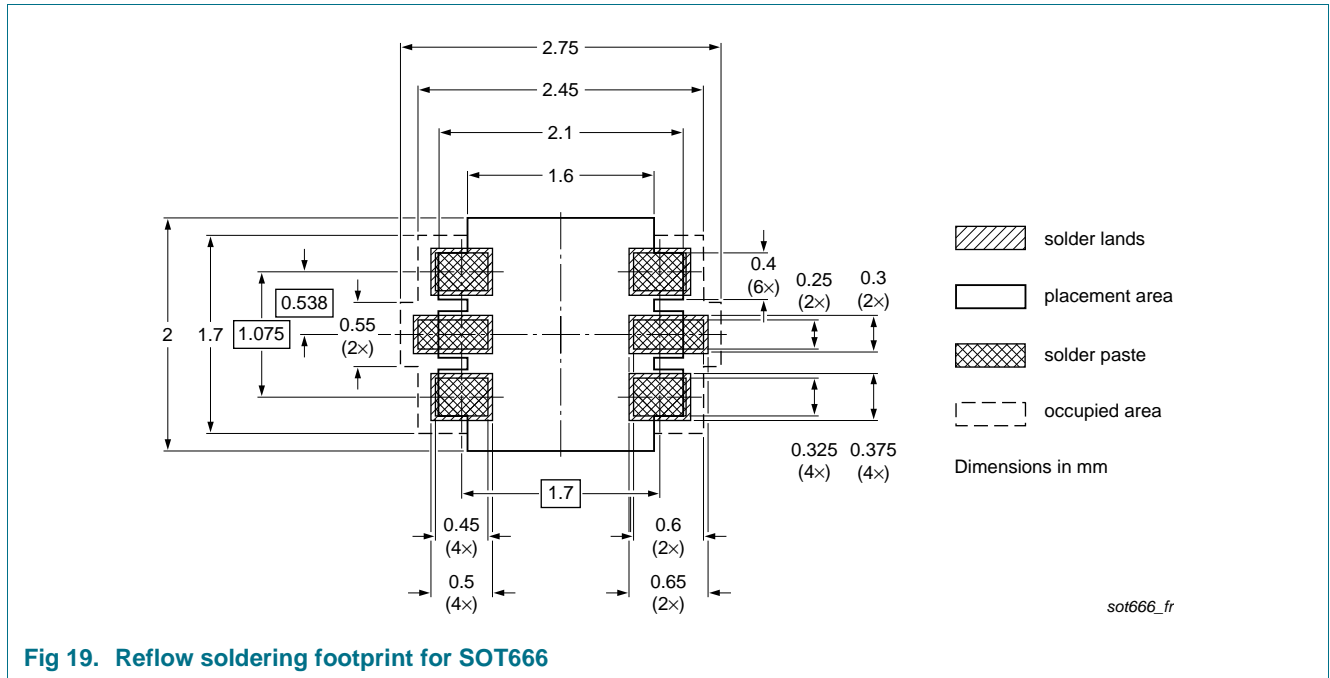
10. Soldering

Fig 19. Reflow soldering footprint for SOT666

11. Revision history

Table 8. **Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMDT290UNE v.1	20110913	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1]   Please consult the most recently issued document before initiating or completing a design.

[2]   The term 'short data sheet' is explained in section "Definitions".

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