Tagus Artix 7 PCI Express Development Board

by Numato Lab Help Center

1. Introduction

<IMAGE>

Tagus is an easy to use FPGA Development Board featuring Xilinx Artix-7 FPGA with x1 PCIe interface, TPM – SPI interface, SFP+ connectors, and 2GB DDR3 SDRAM. This board features Xilinx XC7A100T– FGG484 FPGA. The board features Low Pin Count (LPC) high-speed FMC connector conforming to **ANSI/VITA 57.1 Standard** for the purpose of adding additional features to the board by using custom or commercial off-the-shelf daughter boards.

Applications:

- Parallel Processing and Accelerators
- Product Prototype Development
- Development and Testing of custom embedded processors
- Signal Processing
- Communication Devices Development
- Data Acquisition
- Educational tool for Schools and Universities

Board features

- FPGA: Artix-7 XC7A100T in -1 FGG484 package
- 1 lane PCIe Gen1.0 (2.5GT/s)
- DDR3: 2Gb DDR3 (MT41J128M16HA-125:K or equivalent)
- 128 Mb QSPI flash memory (N25Q128A13ESE40E) for Configuration and optional data storage
- USB to UART serial converter
- 1 x 100MHz CMOS oscillator
- Maximum 76 IOs for user-defined purposes on ANSI/VITA 57.1 Standard compliant FMC LPC connector
- 1x GTP lanes upto 2.5Gbps on **ANSI/VITA 57.1 Standard** compliant FMC LPC connector
- 1 RGB LED for custom use
- 1x TPM – SPI Interface
- 2x SFP+ Cages
- MicroSD adapter for bulk data storage
- Onboard voltage regulators for single power rail operation
- Can be powered from PCIe slot or from an external power supply
- JTAG header for programming and debugging
- All differential pairs are length matched on the board

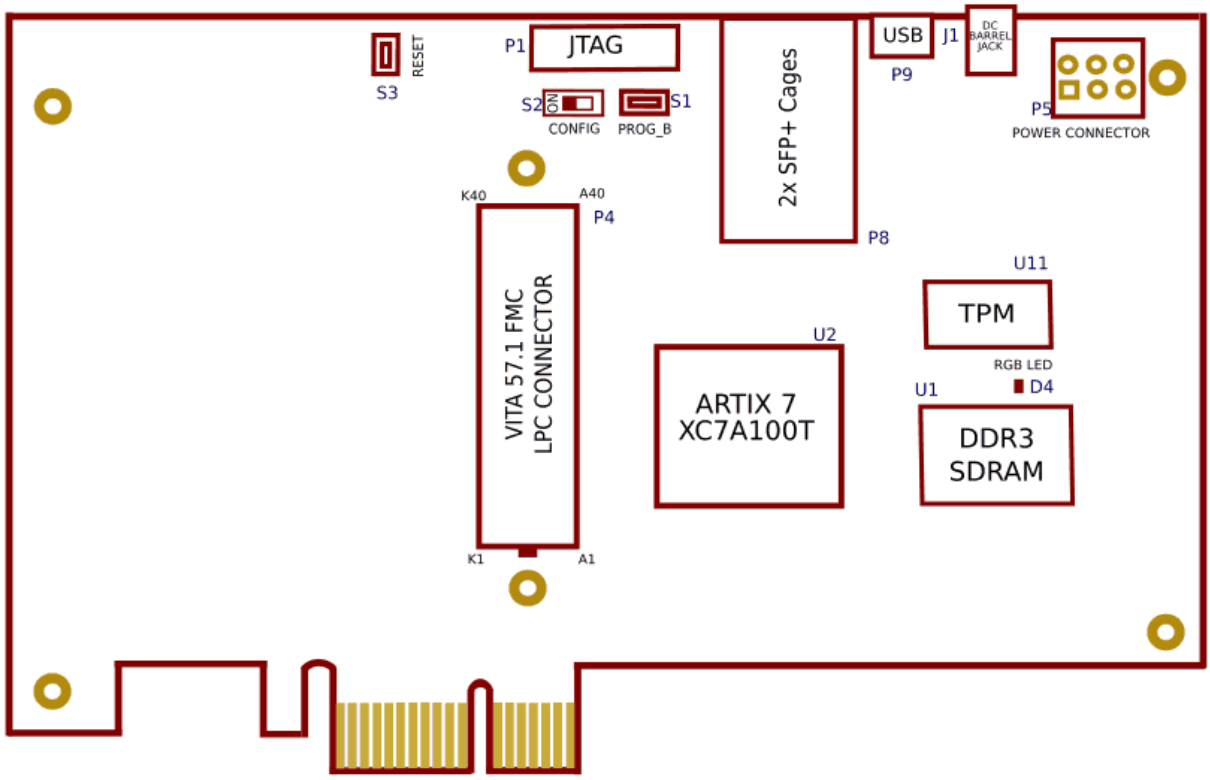
2. How to Use Tagus Artix 7 PCI Express Development Board

2.1. Hardware Accessories Required

Along with the board, following accessories are required for easy and fast installation.

1. 12 V DC Power Supply (not needed if the board is inserted into a motherboard)
2. A Xilinx Platform Cable USB II compatible JTAG programmer
3. USB Male A to Micro B cable (optional)

2.2. Connection Diagram



(https://numato.com/help/wp-content/uploads/2018/05/tagus_connection_diagram.png)

2.3. Power

The Tagus requires +12V power supply to function properly. Tagus can be supplied power in 3 ways:

1. External +12V power via DC Barrel Jack Connector
2. External +12V power via 3×2 PCIe Power Connector.
3. Via Motherboard when the Tagus is plugged into a PCIe slot that is capable of powering the Tagus

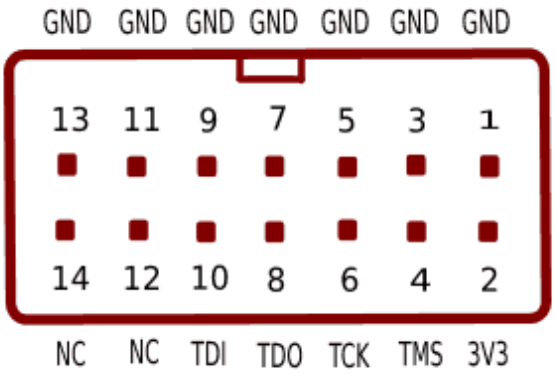
The current requirement for this board largely depends on your application. The Tagus module works on power supply of 1 A of current for simple applications. However, a power supply 2 A of current is recommended for a smooth running of bigger applications. Please consult FPGA data sheet for more details on power requirements.

2.4. USB Serial Bridge

USB Serial Bridge can be used to interface with PC using serial interface. It is primarily used to output debug information or as a console for the design running on the board. <IMAGE> A Micro USB type cable should be used to connect Tagus to host PC. An FT234 is used as the USB-Serial Bridge IC. The USB-Serial interface features hardware flow control using RTS and CTS signals, in case users need to use hardware flow control. An extra signal CBUS0 from FT234X is also connected to FPGA, which can be used as host-controlled GPIO or can be used for other purpose.

2.5. JTAG

JTAG connector allows the FPGA's JTAG registers to be accessed using a JTAG cable compatible with Xilinx Platform Cable USB. Use this header to attach JTAG cable for programming and debugging.



(https://numato.com/help/wp-content/uploads/2018/05/tagus_jtag.png)

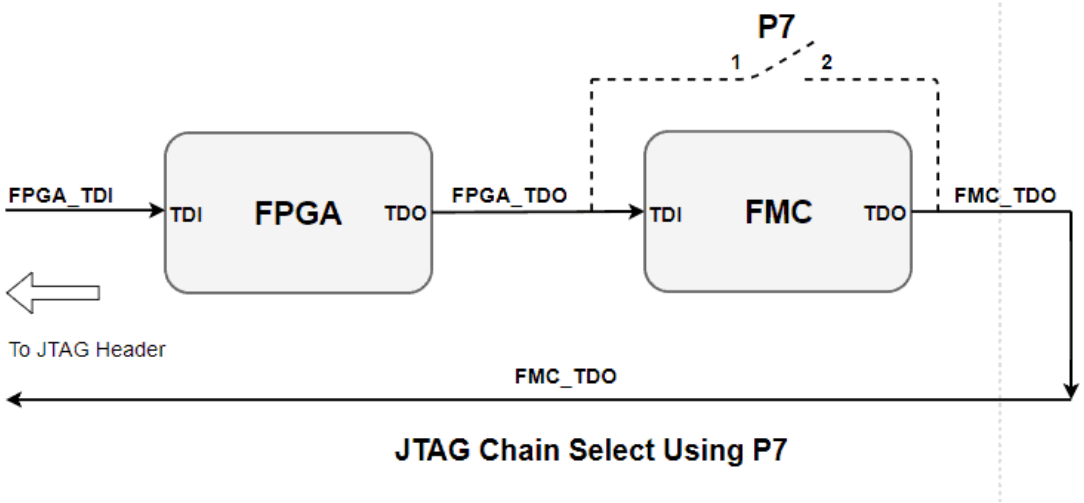
2.6. RGB LED

Tagus features one RGB LED which can be used for custom or debug purposes. The LED is wired in active-low configuration.

2.7. JTAG Chain Configuration

JTAG chain can be modified using jumper P7 near JTAG header.

Following diagram shows JTAG chain



(https://numato.com/help/wp-content/uploads/2018/05/tagus_jtag_chain.png)

Tagus has automatic FMC detection using PRSNT_M2C_L signal from FMC. Normally, when an FMC board is not connected, the Tagus's onboard circuitry will automatically close the JTAG chain keeping FMC out from the chain, so no user intervention is required. But, still jumper P7 has been provided as a redundant backup to close configuration.

the JTAG chain in case the automatic circuitry doesn't work due to non-compliant FMC modules connected to the Tagus, or any or unforeseen reasons.

2.8. Configuration Mode Switch

FPGA startup configuration mode can be selected using switch S2.

<IMAGE>

Sliding it to ON puts FPGA in "JTAG" configuration mode. Sliding it to OFF puts the FPGA to "Master SPI" configuration mode.

2.9. PROG_B and Reset Buttons

PROG_B Button

Tagus features a Push-button **S1** normally meant to be used as "PROG_B" signal for configuration reset. Push-button S1 is connected to FPGA pin **N12.** For enabling manual configuration reset, push-button **S1** connected to GND. The user can reconfigure the FPGA manually, by pressing this push-button S1.

"PROG_B" is active-low input pin (pulled up with 4.7K external resistor) to the FPGA and it controls the configuration logic. When PROG_B pin is de-asserted, resets the FPGA and initializes the new configuration.

Reset Button

Tagus features a Push-button **S3** normally meant to be used as "Reset" signal for designs running on FPGA. Push-button S3 is connected to FPGA pin **P17.** Push-button S3 is **active-high**, and users need to enable FPGA's internal **Pulldown** on the pin P17 to use the pushbutton correctly. This pushbutton can also be used for any other input and is not just limited to be used as a Reset signal.

2.10. FMC VADJ Power Supply

VADJ Power Supply for FMC Bank A is configurable via jumpers J2. Following are the jumper configurations for different voltages for VADJ supply.

Edit(https://numato.com/help/wp-admin/admin.php?page=tablepress&action=edit&table_id=243)

Jumper on J2 Header	FMC VADJ Power Supply (Volts)
No jumper anywhere	3.3
1 - 2	2.5
3 - 4	1.8
5 - 6	1.5
7 - 8	1.2

2.11. PCIe x1 Edge Connector

PCI Express 1.0 1-lane edge-connector on Tagus can be used to interface with host PCs via PCI Express protocol. Each lane is capable of 2.5 GT/s resulting in maximum theoretical data transfer rate of 250 MB/s for a single lane.

PCI Express x1 Edge Connector

Signal Name	Artix-7 (FGG484) Pin

Edit(https://numato.com/help/wp-admin/admin.php?page=tablepress&action=edit&table_id=244)

Signal Name	Artix-7 (FGG484) Pin
PCIE_TX0_P	B4
PCIE_TX0_N	A4
PCIE_RX0_P	B8
PCIE_RX0_N	A8
PCIE_CLK0_P	F6
PCIE_CLK0_N	E6
PCIE_PERST	W20

2.12. FMC Connector

Tagus features a high speed, low pin-count FMC connector which can be used to provide additional features and capabilities to it using custom or commercial off-the-shelf daughter boards. Apart from IOs, 1 GTP lane is available via FMC connector for custom purpose.

FMC Banks A to D

Edit(https://numato.com/help/wp-admin/admin.php?page=tablepress&action=edit&table_id=245)

A	FMC Pin Name	Artix-7 FGG484 Pin	B	FMC Pin Name	Artix-7 FGG484 Pin	C	FMC Pin Name	Artix-7 FGG484 Pin	D	FMC Pin Name	Artix-7 FGG484 Pin
C1	GND	GND	D1	PG_C2M	V20	G1	GND	GND	H1	VREF_A_M2C	NC
C2	DP0_C2M_P	D5	D2	GND	GND	G2	CLK1_M2C_P	K18	H2	PRSNT_M2C_L	W17
C3	DP0_C2M_N	C5	D3	GND	GND	G3	CLK1_M2C_N	K19	H3	GND	GND
C4	GND	GND	D4	GBTCLK0_M2C_P	F10	G4	GND	GND	H4	CLK0_M2C_P	C18
C5	GND	GND	D5	GBTCLK0_M2C_N	E10	G5	GND	GND	H5	CLK0_M2C_N	C19
C6	DP0_M2C_P	D11	D6	GND	GND	G6	LA00_CC_P	D17	H6	GND	GND
C7	DP0_M2C_N	C11	D7	GND	GND	G7	LA00_CC_N	C17	H7	LA02_P	E19
C8	GND	GND	D8	LA01_CC_P	J19	G8	GND	GND	H8	LA02_N	D19
C9	GND	GND	D9	LA01_CC_N	H19	G9	LA03_P	F13	H9	GND	GND
C10	LA06_P	J22	D10	GND	GND	G10	LA03_N	F14	H10	LA04_P	F18
C11	LA06_N	H22	D11	LA05_P	L19	G11	GND	GND	H11	LA04_N	E18
C12	GND	GND	D12	LA05_N	L20	G12	LA08_P	F16	H12	GND	GND
C13	GND	GND	D13	GND	GND	G13	LA08_N	E17	H13	LA07_P	B20
C14	LA10_P	H20	D14	LA09_P	N22	G14	GND	GND	H14	LA07_N	A20
C15	LA10_N	G20	D15	LA09_N	M22	G15	LA12_P	C14	H15	GND	GND
C16	GND	GND	D16	GND	GND	G16	LA12_N	C15	H16	LA11_P	A18
C17	GND	GND	D17	LA13_P	M18	G17	GND	GND	H17	LA11_N	A19
C18	LA14_P	K21	D18	LA13_N	L18	G18	LA16_P	E13	H18	GND	GND
C19	LA14_N	K22	D19	GND	GND	G19	LA16_N	E14	H19	LA15_P	F19
C20	GND	GND	D20	LA17_C	B17	G20	GND	GND	H20	LA15_N	F20

A	FMC Pin Name	Artix-7 FGG484 Pin	B	FMC Pin Name	Artix-7 FGG484 Pin	C	FMC Pin Name	Artix-7 FGG484 Pin	D	FMC Pin Name	Artix-7 FGG484 Pin
				C_P							
C21	GND	GND	D21	LA17_CC_N	B18	G21	LA20_P	E16	H21	GND	GND
C22	LA18_CC_P	J20	D22	GND	GND	G22	LA20_N	D16	H22	LA19_P	D20
C23	LA18_CC_N	J21	D23	LA23_P	N18	G23	GND	GND	H23	LA19_N	C20
C24	GND	GND	D24	LA23_N	N19	G24	LA22_P	D14	H24	GND	GND
C25	GND	GND	D25	GND	GND	G25	LA22_N	D15	H25	LA21_P	C22
C26	LA27_P	M21	D26	LA26_P	N20	G26	GND	GND	H26	LA21_N	B22
C27	LA27_N	L21	D27	LA26_N	M20	G27	LA25_P	B15	H27	GND	GND
C28	GND	GND	D28	GND	GND	G28	LA25_N	B16	H28	LA24_P	B21
C29	GND	GND	D29	FMC_TCK	V12	G29	GND	GND	H29	LA24_N	A21
C30	FMC_SCL	N13	D30	FPGA_TDO_FMC_TDI	U13	G30	LA29_P	C13	H30	GND	GND
C31	FMC_SDA	N14	D31	FMC_TDO	R13	G31	LA29_N	B13	H31	LA28_P	E22
C32	GND	GND	D32	3P3VAUX	VCC3V3	G32	GND	GND	H32	LA28_N	D22
C33	GND	GND	D33	FMC_TMS	T13	G33	LA31_P	A15	H33	GND	GND
C34	GA0	GND	D34	TRST_L	NC	G34	LA31_N	A16	H34	LA30_P	E21
C35	12P0V	VCC12V0	D35	GA1	GND	G35	GND	GND	H35	LA30_N	D21
C36	GND	GND	D36	3P3V	VCC3V3	G36	LA33_P	A13	H36	GND	GND
C37	12P0V	VCC12V0	D37	GND	GND	G37	LA33_N	A14	H37	LA32_P	G21
C38	GND	GND	D38	3P3V	VCC3V3	G38	GND	GND	H38	LA32_N	G22
C39	3P3V	VCC3V3	D39	GND	GND	G39	VADJ	VCC_VADJ	H39	GND	GND
C40	GND	GND	D40	3P3V	VCC3V3	G40	GND	GND	H40	VADJ	VCC_VADJ

3. USB-Serial Bridge Driver

3.1. Installing Driver for USB Serial Converter on Windows

This board requires a driver to be installed to use USB serial converter, for board’s proper functioning when used with Windows. Ideally, Windows should automatically search and install the correct driver for Tagus via Windows Update. For manual installation, the FTDI VCP drivers are available for download from http://www.ftdichip.com/(http://www.ftdichip.com/)
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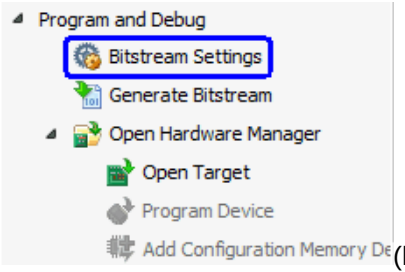
4. Generating Bitstream Using Vivado

The PCI Express specification requires cards to be ready for link training within 100 ms after the host PC's power supply is stable.

Following constraints need to be added to the xdc file before synthesizing, implementing and generating a bitstream for a PCI Express design. These can be safely ignored if PCI Express interface is not used in the design.

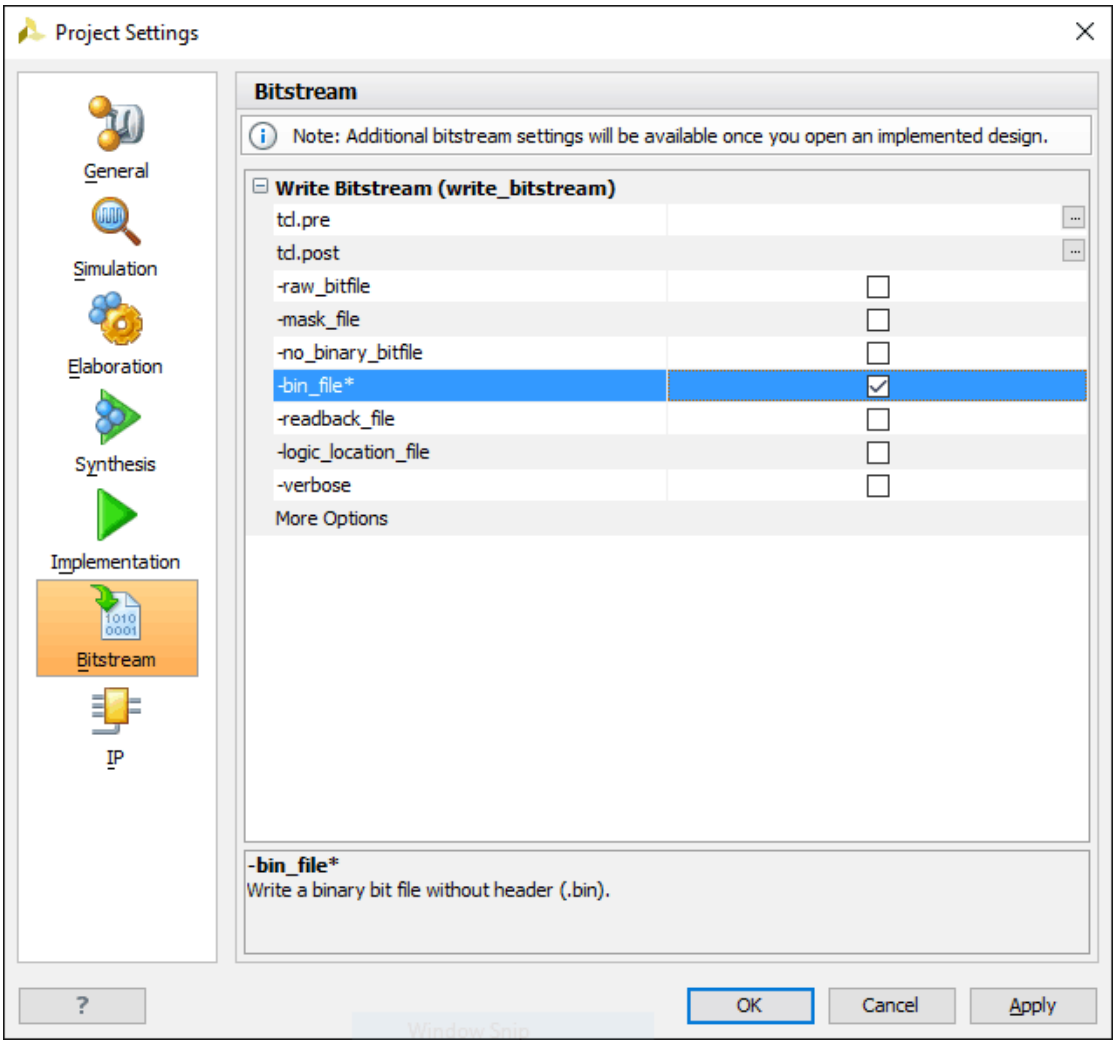
```
set_property BITSTREAM.CONFIG.CONFIGRATE 66 [current_design]
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 4 [current_design]
```

Step 1: It is recommended to generate .bin bitstream file along with .bit bitstream file. Click "Bitstream Settings".



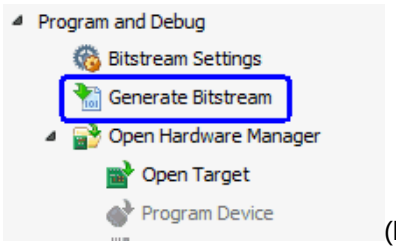
(https://numato.com/help/wp-content/uploads/2016/10/vivado_bitstream_settings_location.png)

Step 2: Select "-bin_file*" option in the dialog window and Click OK.



(https://numato.com/help/wp-content/uploads/2016/10/vivado_bitstream_settings.png)

Step 3: Finally click “Generate Bitstream”.



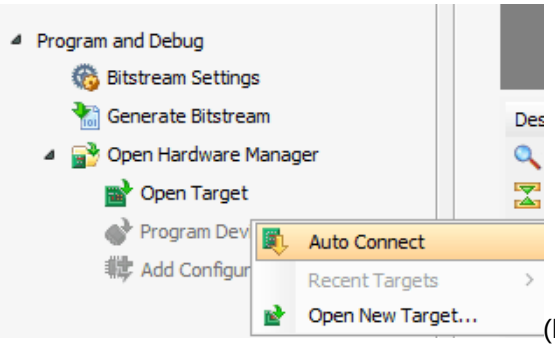
(https://numato.com/help/wp-content/uploads/2016/10/vivado_generate_bitstream.png)

5. Programming Tagus Using JTAG

Tagus Artix-7 PCI Express FPGA Board features an onboard JTAG connector which facilitates easy reprogramming of SRAM and onboard SPI flash through JTAG programmer like “Xilinx Platform cable USB”. Following steps illustrate how to program FPGA on Tagus using JTAG.

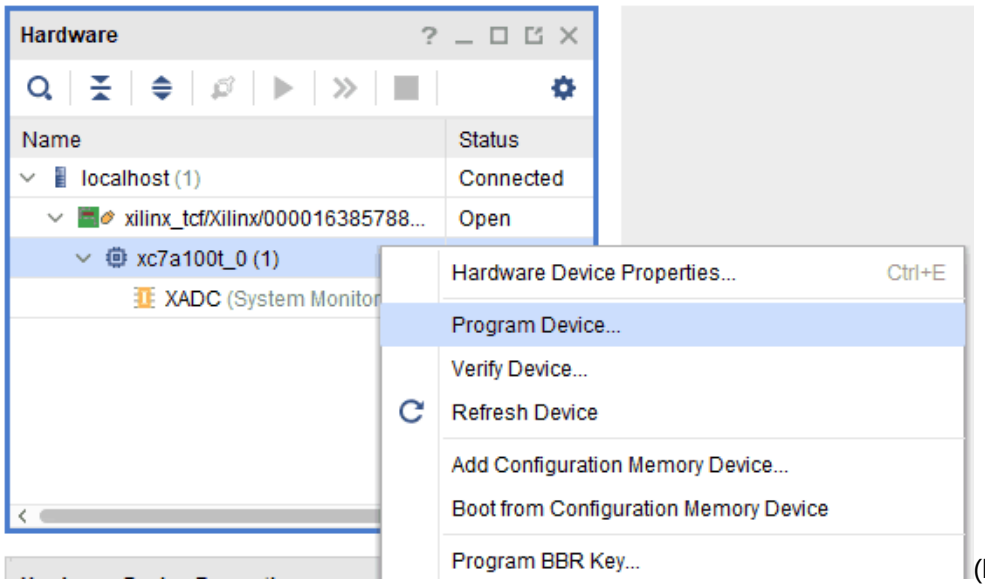
Step1: By using JTAG cable, connect Xilinx platform cable USB to Tagus and power it up.

Step2: Open Vivado project and open the target by clicking on the “Open Target” in “Open Hardware Manager” in the “Program and Debug” section of the Flow Navigator window. Select “Auto Connect”.



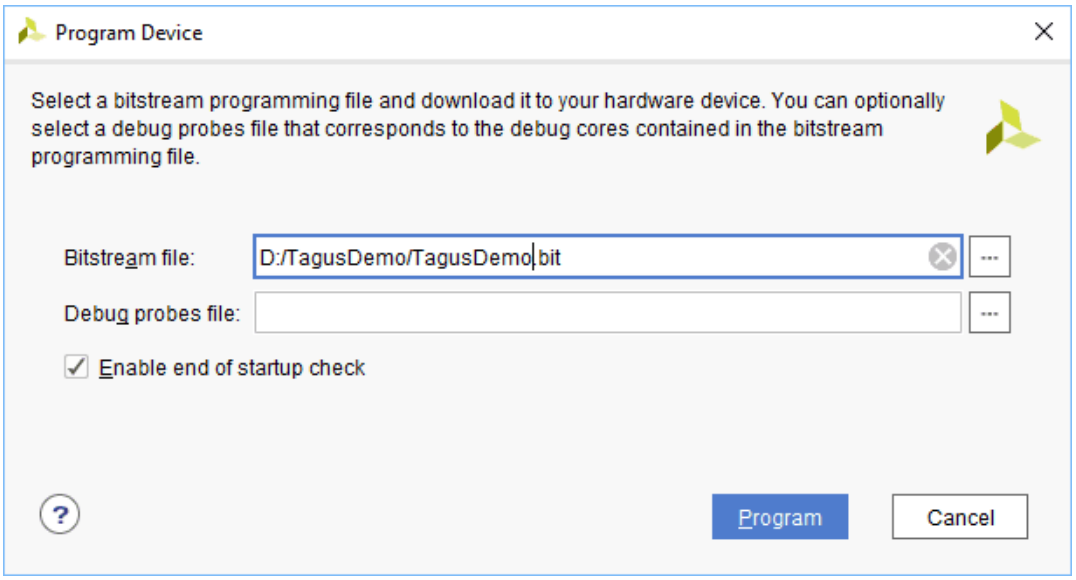
(https://numato.com/help/wp-content/uploads/2016/10/vivado_open_hardware_manager-e1475583576193.png)

Step3: If the device is detected successfully, then select “Program Device” by right click on the target device “xc7a100t_0” as shown below.



(https://numato.com/help/wp-content/uploads/2018/05/vivado_prog_device.png)

Step4: In the dialog window which opens up, Vivado automatically chooses correct bitstream file if the design was synthesized, implemented and bitstream generated successfully. If needed, browse to the bitstream which needs to be programmed to FPGA. Finally, click “Program”.

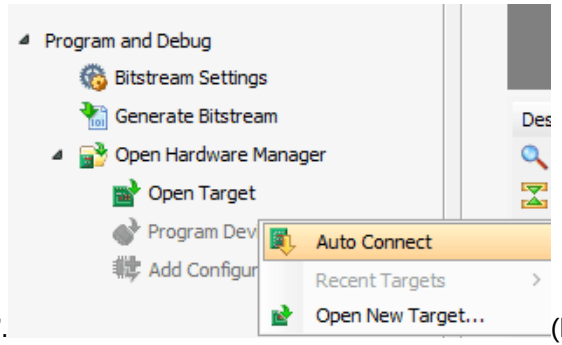


(https://numato.com/help/wp-content/uploads/2018/05/vivado_prog_device_2.png)

As soon as “Program” is clicked, a red colored LED (D1) on Tagus should light up, indicating that programming process is going on. This LED will turn off when the configuration is complete.

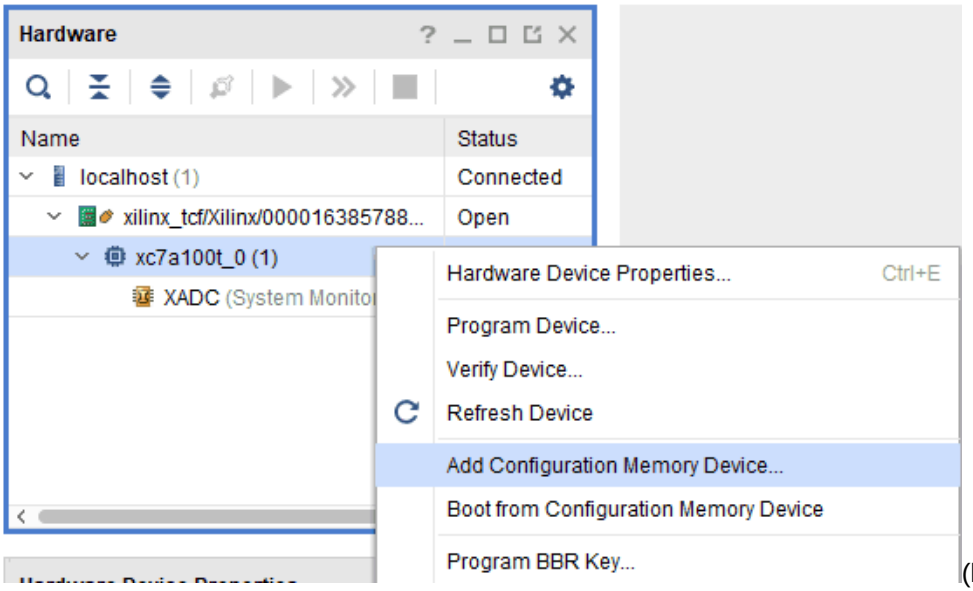
6. Programming QSPI Flash using Vivado

A .bin or .mcs file is required for programming Tagus’s onboard QSPI flash.

Step 1: Open Vivado project and open the target by clicking on the “Open Target” in “Open Hardware Manager” in the “Program and Debug” section of the Flow Navigator window. Select
“Auto


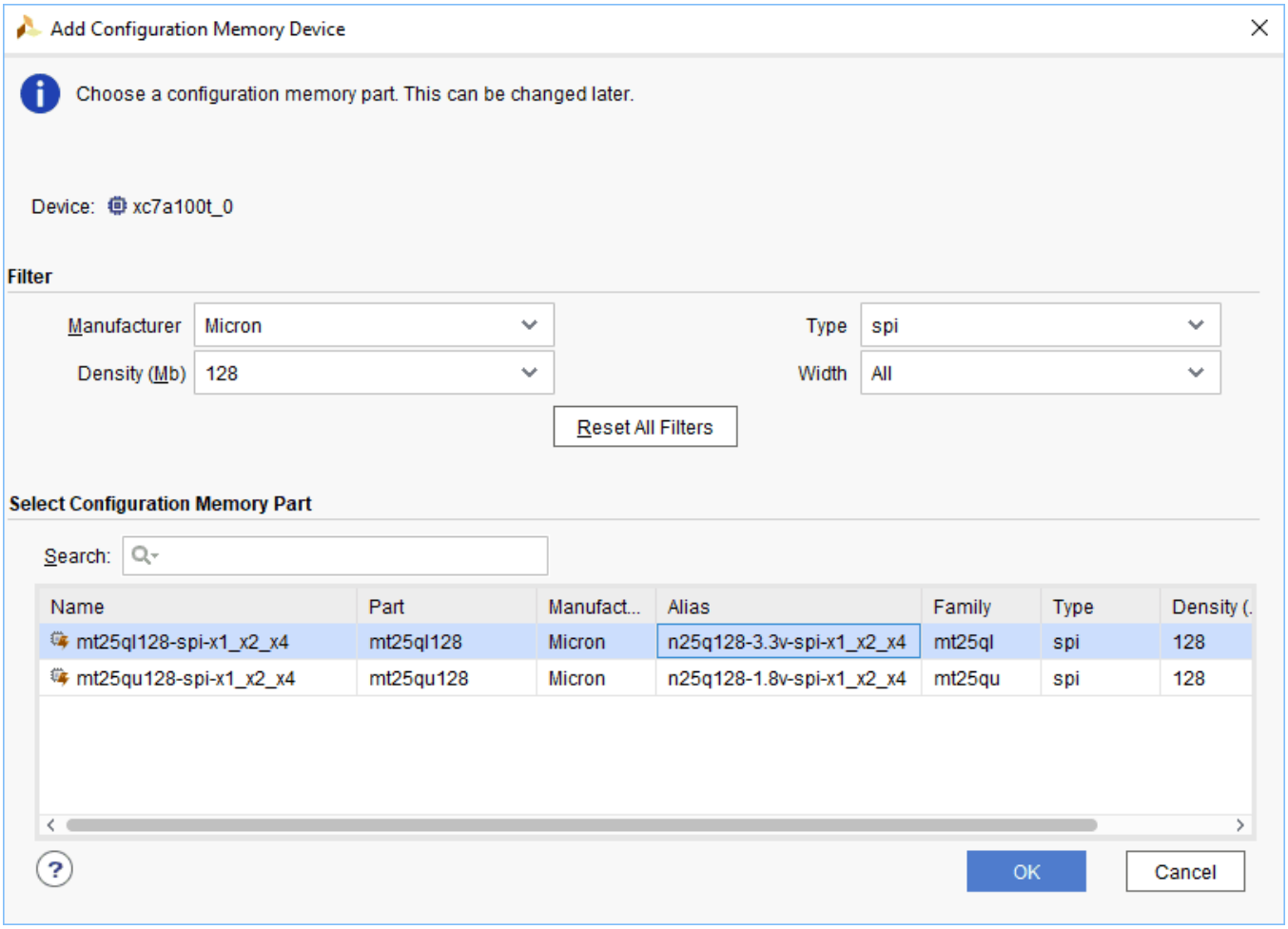
Connect”.(https://numato.com/help/wp-content/uploads/2016/10/vivado_open_hardware_manager-e1475583576193.png)

Step 2: If the device is detected successfully, then select “Add Configuration Memory Device” by right click on the target device “xc7a100t_0” as shown below.



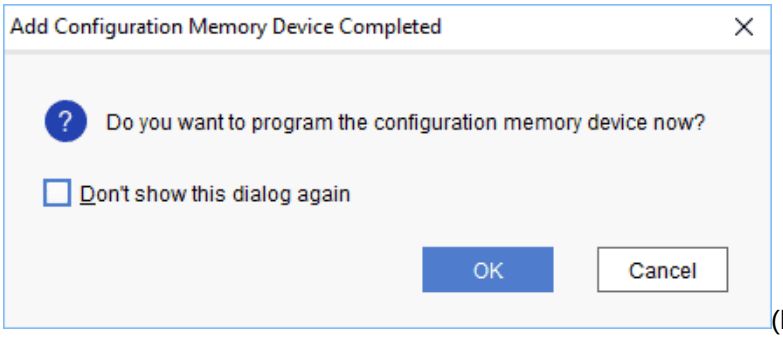
(https://numato.com/help/wp-content/uploads/2018/05/vivado_add_config_mem.png)

Step 3: Select the memory device “mt25ql128-spi-x1_x2_x4 (which is equivalent to n25q128-3.3v-spi-x1_x2_x4)”, then click OK.



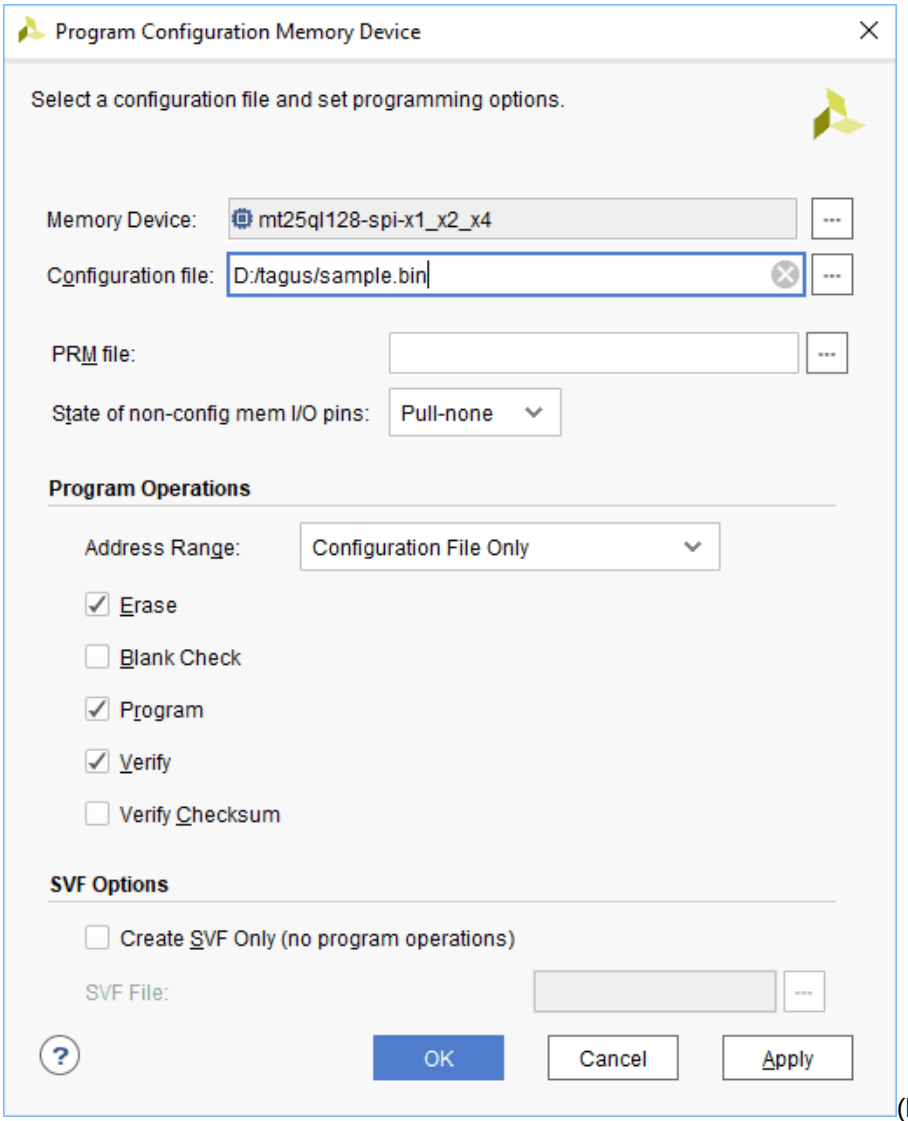
(https://numato.com/help/wp-content/uploads/2018/05/vivado_select_mem_device1.png)

Step 4: After completion of Step 3 the following dialog box will open. Click OK.



(https://numato.com/help/wp-content/uploads/2018/05/vivado_select_mem_device2.png)

Step 5: Browse to the working .bin file or the .mcs file (whichever applicable) and click OK to program as shown below. If programming is successful, a confirmation message will be displayed.



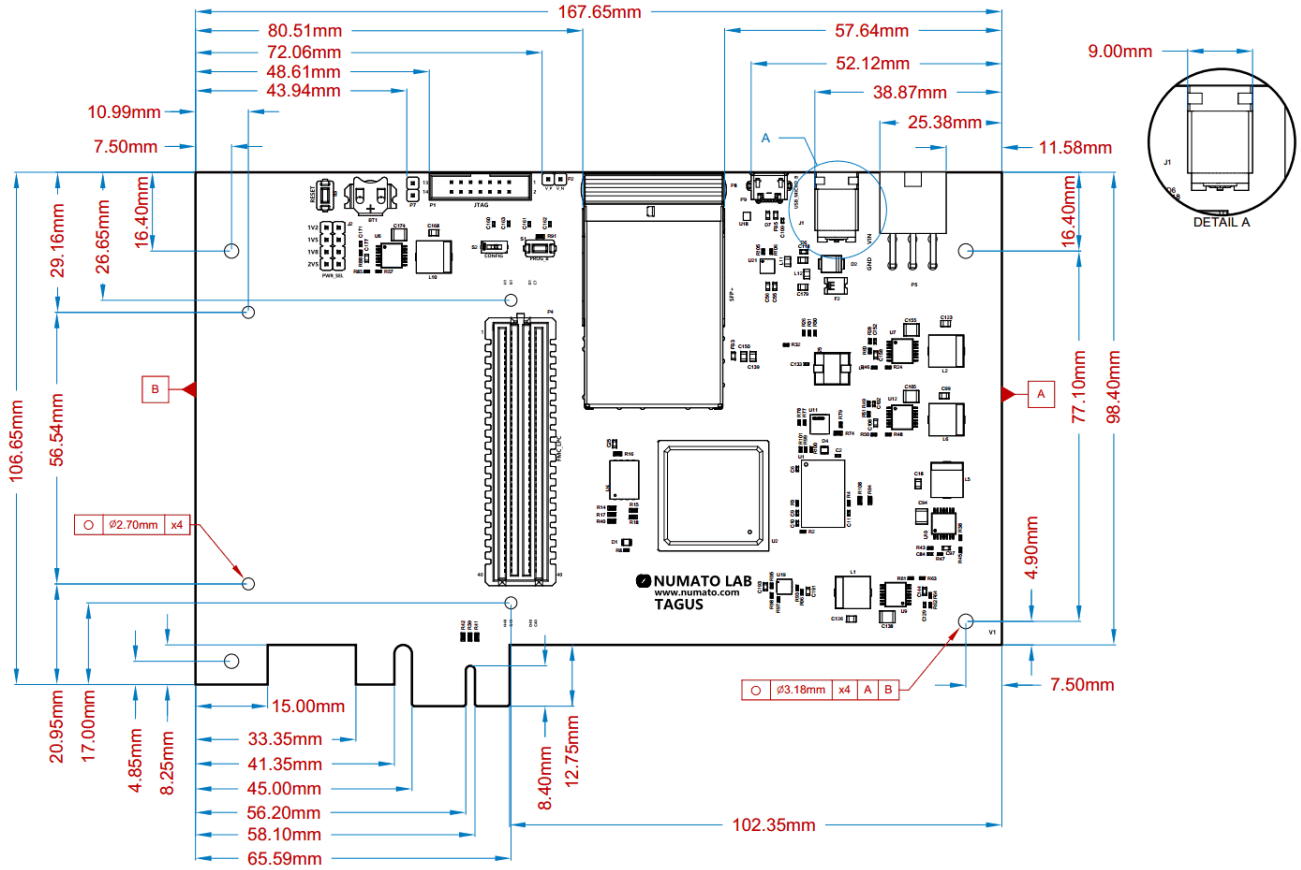
(https://numato.com/help/wp-content/uploads/2018/05/vivado_prog_config_mem_device.png)

7. Technical Specifications

Edit(https://numato.com/help/wp-admin/admin.php?page=tablepress&action=edit&table_id=246)

Parameter *	Value	Unit
Basic Specifications		
Number of GPIOs (Max)	76	
On-board Oscillator Frequency (ASEM1-100.000MHZ-LC-T)	100 (x1)	MHz
DDR3 (MT41J123M16HA-125)	2 (x1)	GB
SPI Flash Memory (N25Q128A13ESE40E)	128	Mb
IIC Eeprom (24AA02E48T-I/OT)	2	Kb
FPGA Specifications		
Internal supply voltage relative to GND	-0.5 to 1.1	V
Auxiliary supply voltage relative to GND	-0.5 to 2.0	V
Output drivers supply voltage relative to GND	-0.5 to 3.6	V
Connector Header Specifications (ASP-134603-01)		
Number of Positions	160	
Number of Rows	4	
Height above Board	6.55	mm
Pitch	1.27	mm
Mated Receptacle on Tagus module	ASP-134603-01	

8. Mechanical Dimensions



(https://numato.com/help/wp-content/uploads/2018/05/TagusPd.pdf)

9. Vivado XDC Constraints

Download Tagus Constraints for Vivado <LINK>

10. Schematics

Tagus V1.0 Schematics(https://numato.com/help/wp-content/uploads/2018/05/TagusSchematic.pdf)

11. Tagus FMC Easy Reference

Tagus FMC Easy Reference(https://numato.com/help/wp-content/uploads/2018/05/Tagus_FMC_Easy_Reference.pdf)