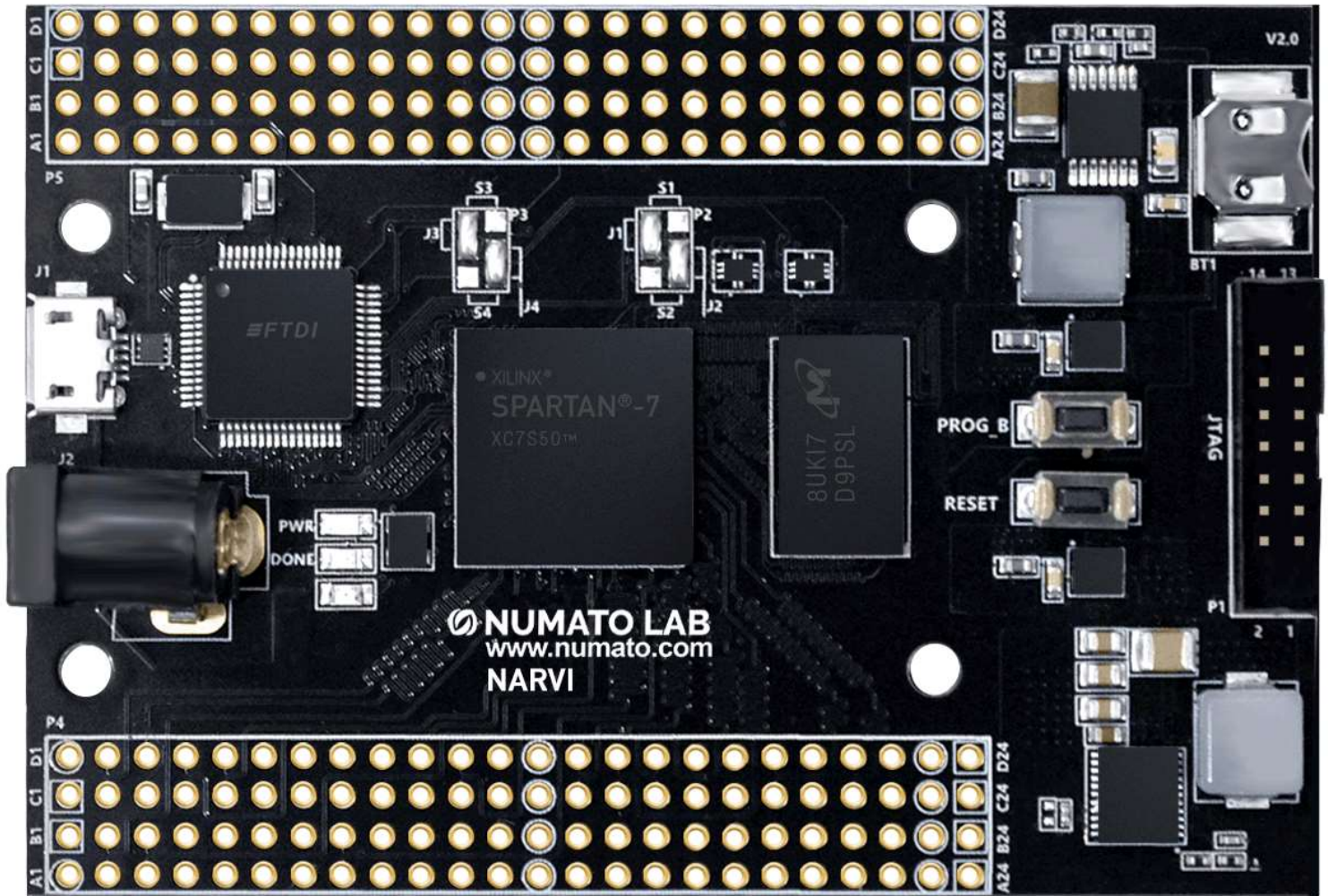


Introduction



(https://numato.com/help/wp-content/uploads/2018/06/Narvi_1200x1200-1.png)

Narvi is an easy to use FPGA Development board featuring Spartan 7 FPGA (XC7S50 – CSG324A package) with FTDI's FT2232H Dual-Channel USB device. It is specially designed for the development and integration of FPGA based accelerated features to other designs. The Narvi – Spartan 7 FPGA Board (<https://numato.com/product/narvi-spartan-7-fpga-module>) is pin compatible with Saturn Spartan 6 FPGA Module (<https://numato.com/saturn-spartan-6-fpga-development-board-with-ddr-sdram/>), Skoll Kintex 7 FPGA Module (<https://numato.com/product/skoll-kintex-7-fpga-development-board/>), Neso Artix 7 FPGA Module (<https://numato.com/neso-artix-7-fpga-development-board/>), Styx Zynq 7020 FPGA Module (<https://numato.com/product/styx-zynq-7020-fpga-module>) and Telesto MAX10 FPGA Module (<https://numato.com/product/telesto-max10-fpga-module>) and thus offers a seamless upgrade path. The high-speed USB 2.0 interface provides fast and easy configuration download to the onboard SPI flash. No programmer or special downloader cable is needed to download the bit stream to the board. The second FTDI channel can be used to develop custom high data-rate USB based applications. Narvi provides user flexibility in adding their own peripherals through IO Expansion Headers.

Board Features

- Pin compatible with Saturn Spartan 6 FPGA Module (<https://numato.com/saturn-spartan-6-fpga-development-board-with-ddr-sdram/>), Skoll Kintex 7 FPGA Module (<https://numato.com/product/skoll-kintex-7-fpga-development-board>), Neso Artix 7 FPGA Module (<https://numato.com/neso-artix-7-fpga-development-board/>), Styx Zynq 7020 FPGA Module (<https://numato.com/product/styx-zynq-7020-fpga-module>) and Telesto MAX10 FPGA Module (<https://numato.com/product/telesto-max10-fpga-module>) and offers a seamless upgrade path
- FPGA: XC7S50 in CSGA324 package, Speed Grade: -1
- DDR3: 2Gb DDR3 (MT41J128M16HA-125:K or equivalent)
- Flash memory: 128 Mb Quadbit SPI flash memory (N25Q128A13ESE40E)
- 100MHz CMOS oscillator
- High-Speed USB 2.0 interface for On-board flash programming. FT2232H Channel B is dedicated for SPI Flash /JTAG Programming. Channel A can be used for custom applications.
- Onboard voltage regulators for single power rail operation
- FPGA configuration via JTAG and USB
- Maximum IOs for user-defined purposes
 - FPGA – 130 IOs
 - FT2232H – 8 IOs

Applications

- Product Prototype Development
- Accelerated computing integration
- Development and testing of custom embedded processors
- Signal Processing
- Communication devices development
- Educational tool for Schools and Universities

How to use Narvi Spartan 7 FPGA Module

The following sections describe in detail how to use this module.

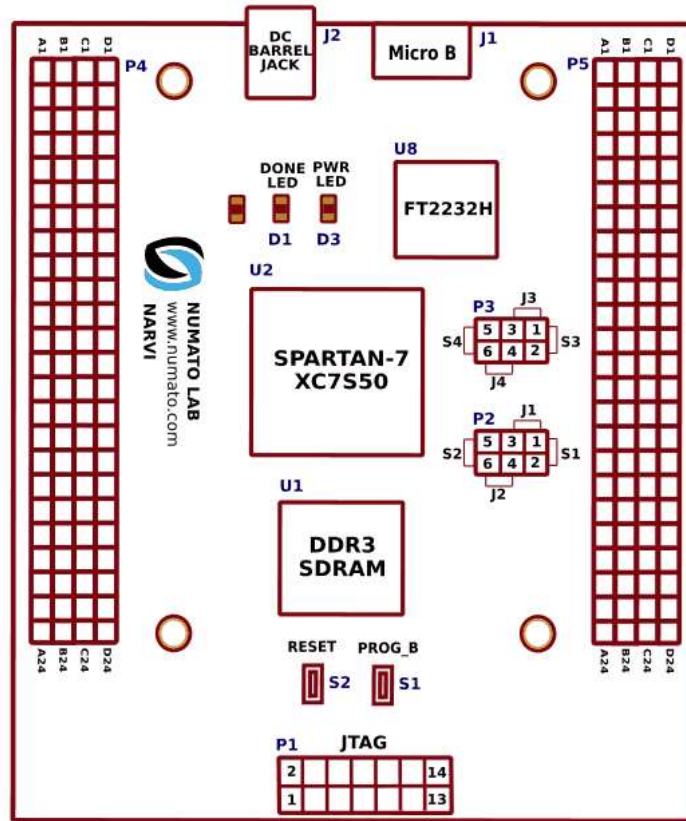
Hardware Accessories Required

For easy and fast installation, you may need the following items along with the Narvi module.

- USB A to Micro B cable
- DC Power supply
- A Xilinx Platform Cable USB II compatible JTAG programmer (optional)

Connection Diagram

The following connection diagram should be used for reference only. The schematics are available at the end of this document for detailed information.



(<https://numato.com/help/wp-content/uploads/2018/06/narvi-connection-diagram.png>)

USB Interface

The onboard high speed USB controller helps a PC/Linux/Mac computer to communicate with this module. Use a USB A to Micro B cable to connect with a PC. (https://numato.com/help/wp-content/uploads/2018/06/narvi_usb.png)

By default, the module is powered by USB so make sure not to overcrowd unpowered USB hubs (the picture on the right shows Micro B connector)



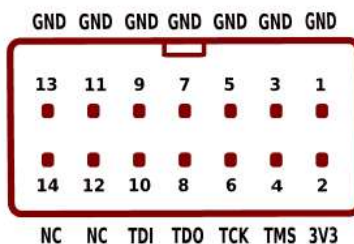
DC Power Supply

(https://numato.com/help/wp-content/uploads/2018/06/narvi_power.png)The board is configured to use power from DC power supply by connecting it to the External DC Jack. Please refer to the marking on the board for more details. The external power supply should be in the range of +7 to +12V, with sufficient current rating.



JTAG Connector

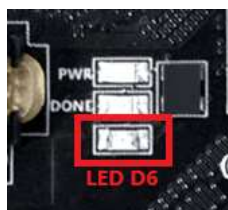
JTAG connector allows the FPGA's JTAG registers to be accessed using a JTAG cable, compatible with Xilinx Platform Cable USB. Use this header, to attach JTAG cable for programming and debugging.



(https://numato.com/help/wp-content/uploads/2018/06/narvi_jtag.png)

Reset Button and LED

Narvi S7 features a Push-button **S2** normally meant to be used as “Reset” signal for designs running on FPGA. Push-button S2 is connected to FPGA pin **T14**. Push-button S2 is **active-high**. This push button can also be used for any other input and is not just limited to be used as a Reset signal.



(https://numato.com/help/wp-content/uploads/2019/02/D6_LED.png)

Narvi S7 also features a general purpose LED **D6** which can be used in the RTL design as per requirement. LED D6 is connected to FPGA pin **G13**. LED D6 is **active-low**.

PROG_B Button

Narvi features a Push-button **S1** normally meant to be used as “PROG_B” signal for configuration reset. Push-button S1 is connected to FPGA pin **R8**. For enabling manual configuration reset, push-button **S1** is connected to GND. The user can reconfigure the FPGA manually, by pressing this push-button S1.

“PROG_B” is active-low input pin (pulled up with 4.7K external resistor) to the FPGA and it controls the configuration logic. An assertion followed by de-assertion cycle on PROG_B pin resets the FPGA and initializes the new configuration.

JTAG/SPI Configuration on FT2232H Channel B

Channel B of FT2232H can be connected to the SPI bus that connects the SPI Flash chip to the FPGA or to the JTAG pins of the FPGA. When FT2232H channel B is connected to FPGA JTAG, the JTAG signals can be accessed directly through FT2232H. This is the default configuration set when Narvi S7 is shipped.

Please see the tables below for information about selecting SPI or JTAG for FT2232H channel B.

Solder Jumpers P2

Jumper Configuration for SPI	Jumper Configuration for JTAG
1 - 2 (S1)	1 - 3 (J1)
5 - 6 (S2)	4 - 6 (J2)

Solder Jumpers P3

Jumper Configuration for SPI	Jumper Configuration for JTAG
1 - 2 (S3)	1 - 3 (J3)
5 - 6 (S4)	4 - 6 (J4)

By default, Narvi S7 ships with the solder jumpers in JTAG configuration. During normal usage, users should not change these jumpers from their factory default configuration.

GPIOs

This device is equipped with a maximum 130 user IO pins that can be used for various custom applications. All user IOs are length matched and can be used as differential pairs.

Header P4

Pin No. On The Header	GPIO Pin Name	Spartan-7 (CSGA324) Pin No.	Pin No. On The Header	GPIO Pin Name	Spartan-7 (CSGA324) Pin No.	Pin No. On The Header	GPIO Pin Name	Spartan-7 (CSGA324) Pin No.	Pin No. On The Header	GPIO Pin Name	Spartan-7 (CSGA324) Pin No.
A1		GND	B1		VCC3V3	C1		VIN	D1		GND
A2	GPIO_1_N	A14	B2	GPIO_1_P	B14	C2	GPIO_4_N	A16	D2	GPIO_4_P	B16
A3	GPIO_28_N	A9	B3	GPIO_28_P	A10	C3	GPIO_3_N	A15	D3	GPIO_3_P	B15
A4	GPIO_5_N	A17	B4	GPIO_5_P	B17	C4	GPIO_25_N	A11	D4	GPIO_25_P	B11
A5	GPIO_21_N	C14	B5	GPIO_21_P	C13	C5	GPIO_20_N	A13	D5	GPIO_20_P	B13
A6	GPIO_23_N	D12	B6	GPIO_23_P	E12	C6	GPIO_33_N	G6	D6	GPIO_33_P	H6
A7	GPIO_14_N	D6	B7	GPIO_14_P	E6	C7	GPIO_26_N	F5	D7	GPIO_26_P	G5
A8	GPIO_8_N	A4	B8	GPIO_8_P	A5	C8	GPIO_12_N	C7	D8	GPIO_12_P	D7
A9	GPIO_15_N	D5	B9	GPIO_15_P	E5	C9	GPIO_13_N	A6	D9	GPIO_13_P	B7
A10	GPIO_7_N	B5	B10	GPIO_7_P	C5	C10		NC	D10		NC
A11		NC	B11		NC	C11	GPIO_6_N	A7	D11	GPIO_6_P	A8
A12		NC	B12		NC	C12	GPIO_18_N	E4	D12	GPIO_18_P	F4
A13		GND	B13		GND	C13		GND	D13		GND
A14		NC	B14		NC	C14	GPIO_19_N	A2	D14	GPIO_19_P	A3
A15	GPIO_2_N	B2	B15	GPIO_2_P	C2	C15	GPIO_27_N	F1	D15	GPIO_27_P	F2
A16	GPIO_11_N	D1	B16	GPIO_11_P	E1	C16	GPIO_10_N	B1	D16	GPIO_10_P	C1
A17		NC	B17		NC	C17		NC	D17		NC
A18	GPIO_16_N	B4	B18	GPIO_16_P	C4	C18	GPIO_17_N	B3	D18	GPIO_17_P	C3
A19		NC	B19		NC	C19	GPIO_30_N	G1	D19	GPIO_30_P	G2
A20	GPIO_22_N	D2	B20	GPIO_22_P	E2	C20	GPIO_24_N	E3	D20	GPIO_24_P	F3
A21	GPIO_31_N	H4	B21	GPIO_31_P	H5	C21	GPIO_32_N	J1	D21	GPIO_32_P	J2
A22	GPIO_29_N	H2	B22	GPIO_29_P	H3	C22	GPIO_9_N	J3	D22	GPIO_9_P	J4
A23		GND	B23		GND	C23		GND	D23		GND
A24		VCC3V3	B24		VCC3V3	C24		VCC3V3	D24		VCC3V3

Header P5

Pin No. On The Header	GPIO Pin Name	Spartan-7 (CSGA324) Pin No.	Pin No. On The Header	GPIO Pin Name	Spartan-7 (CSGA324) Pin No.	Pin No. On The Header	GPIO Pin Name	Spartan-7 (CSGA324) Pin No.	Pin No. On The Header	GPIO Pin Name	Spartan-7 (CSGA324) Pin No.
A1	BCBUS0*		B1	BCBUS1		C1		VCC3V3	D1		GND
A2	BCBUS2		B2	BCBUS3		C2	GPIO_46_P	C17	D2	GPIO_46_N	B18

Pin No. On The Header	GPIO Pin Name	Spartan-7 (CSGA324) Pin No.	Pin No. On The Header	GPIO Pin Name	Spartan-7 (CSGA324) Pin No.	Pin No. On The Header	GPIO Pin Name	Spartan-7 (CSGA324) Pin No.	Pin No. On The Header	GPIO Pin Name	Spartan-7 (CSGA324) Pin No.
A3	BCBUS4		B3	BCBUS5		C3	GPIO_47_P	D16	D3	GPIO_47_N	D17
A4	BCBUS6		B4	BCBUS7		C4	GPIO_49_P	F18	D4	GPIO_49_N	E18
A5	GPIO_37_P	D18	B5	GPIO_37_N	C18	C5	GPIO_54_P	C12	D5	GPIO_54_N	C11
A6	GPIO_35_P	G16	B6	GPIO_35_N	G17	C6	GPIO_43_P	N15	D6	GPIO_43_N	P16
A7	GPIO_36_P	E14	B7	GPIO_36_N	E15	C7	GPIO_44_P	H18	D7	GPIO_44_N	G18
A8	GPIO_34_P	F14	B8	GPIO_34_N	F15	C8	GPIO_48_P	E16	D8	GPIO_48_N	E17
A9	GPIO_50_P	H16	B9	GPIO_50_N	H17	C9	GPIO_41_P	J13	D9	GPIO_41_N	J14
A10	GPIO_51_P	K14	B10	GPIO_51_N	J15	C10	GPIO_40_P	K16	D10	GPIO_40_N	J16
A11	GPIO_52_P	R15	B11	GPIO_52_N	T15	C11	GPIO_39_P	H15	D11	GPIO_39_N	G15
A12		GND	B12		GND	C12		GND	D12		GND
A13		GND	B13		GND	C13		GND	D13		GND
A14	GPIO_64_P	U16	B14	GPIO_64_N	V17	C14	GPIO_61_P	U17	D14	GPIO_61_N	U18
A15	GPIO_42_P	R16	B15	GPIO_42_N	R17	C15	GPIO_45_P	H13	D15	GPIO_45_N	H14
A16	GPIO_62_P	P14	B16	GPIO_62_N	P15	C16	GPIO_53_P	C10	D16	GPIO_53_N	C9
A17	GPIO_63_P	U15	B17	GPIO_63_N	V16	C17	GPIO_57_P	T12	D17	GPIO_57_N	T13
A18	GPIO_56_P	U12	B18	GPIO_56_N	V13	C18	GPIO_38_P	F13	D18	GPIO_38_N	E13
A19	GPIO_59_P	U11	B19	GPIO_59_N	V12	C19	GPIO_55_P	V14	D19	GPIO_55_N	V15
A20	GPIO_58_P	R11	B20	GPIO_58_N	T11	C20	V_P	J10	D20	V_N	K9
A21	GPIO_60_P	P13	B21	GPIO_60_N	R13	C21	TCK	D9	D21	TDO	T8
A22	GPIO_65_P	M14	B22	GPIO_65_N	N14	C22	TDI	R9	D22	TMS	T9
A23	INIT_B	U8	B23		VCC3V3	C23	PROGRAM_B	R8	D23		VCC3V3
A24		GND	B24		GND	C24		GND	D24		GND

* BCBUS0 – BCBUS7 are pins of FTDI FT2232H Dual-Channel USB device.

FT2232H - Spartan-7 (CSGA324) FPGA Connection Details

FTDI Pin No.	Pin Function (245 FIFO)	Spartan 7 (CSGA324) Pin No.
16	FTDI-D0	L13
17	FTDI-D1	N13
18	FTDI-D2	L17
19	FTDI-D3	L18
21	FTDI-D4	M17
22	FTDI-D5	M18
23	FTDI-D6	M16
24	FTDI-D7	N18
26	FTDI-RXF#	P18
27	FTDI-TXE#	P17
28	FTDI-RD#	R18
29	FTDI-WR#	T18

FTDI Pin No.	Pin Function (245 FIFO)	Spartan 7 (CSGA324) Pin No.
30	FTDI-SIWUA	L16
32	FTDI-CLKOUT	R14
33	FTDI-OE#	R12

Driver Installation

Windows

This product requires a driver to be installed for proper functioning when used with Windows. The Numato Lab Narvi S7 driver can be downloaded from here (<https://numato.com/wp-content/uploads/2019/01/Driver.zip>). When driver installation is complete, the module should appear in Tenagra FPGA System Management Software as Narvi Spartan 7 FPGA Module.

Linux

The Linux ships with the drivers required for Narvi S7. It should be enough to run the following two commands in the terminal:

```
>> sudo modprobe ftdi_sio
>> echo 2a19 100D > /sys/bus/usb-serial/drivers/ftdi_sio/new_id
```

Generating Bitstream Using Vivado

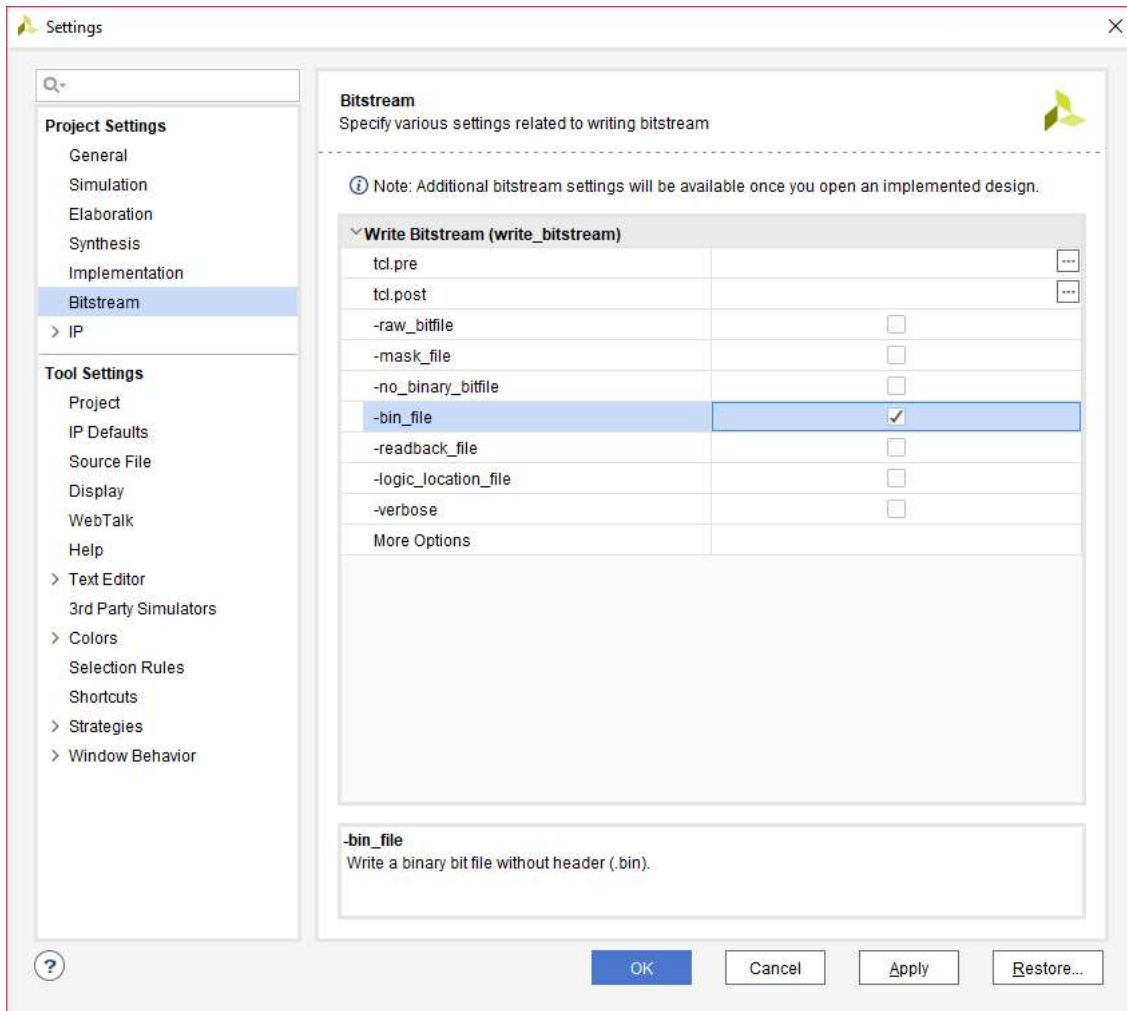
The bitstream can be generated for Narvi in Vivado by following the steps below:

Step 1: It is recommended to generate .bin bitstream file along with .bit bitstream file. Click "Bitstream Settings".



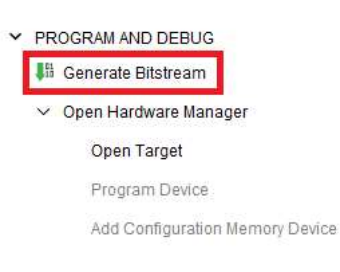
(<https://numato.com/help/wp-content/uploads/2018/05/bitstream-settings.png>)

Step 2: Select "-bin_file*" option in the dialog window and Click OK.



(<https://numato.com/help/wp-content/uploads/2018/05/bitstream-settings1.png>)

Step 3: Finally click "Generate Bitstream".



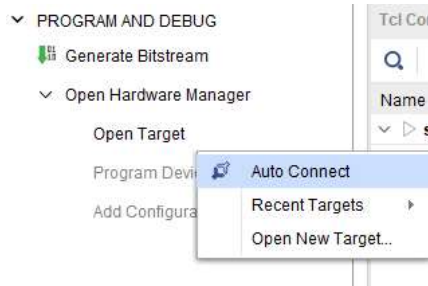
(<https://numato.com/help/wp-content/uploads/2018/05/generatebitstream.png>)

Programming Narvi Using JTAG

Narvi Spartan 7 FPGA Module features an onboard JTAG connector which facilitates easy reprogramming of SRAM and onboard SPI flash through JTAG programmer like "Xilinx Platform cable USB". Following steps illustrate how to program FPGA on Narvi using JTAG.

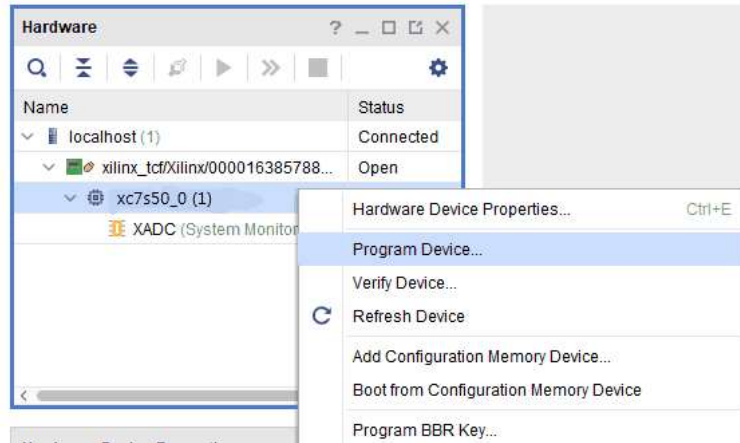
Step 1: By using JTAG cable, connect Xilinx platform cable USB to Narvi and power it up.

Step 2: Open Vivado project and open the target by clicking on the "Open Target" in "Open Hardware Manager" in the "Program and Debug" section of the Flow Navigator window. Select "Auto Connect".



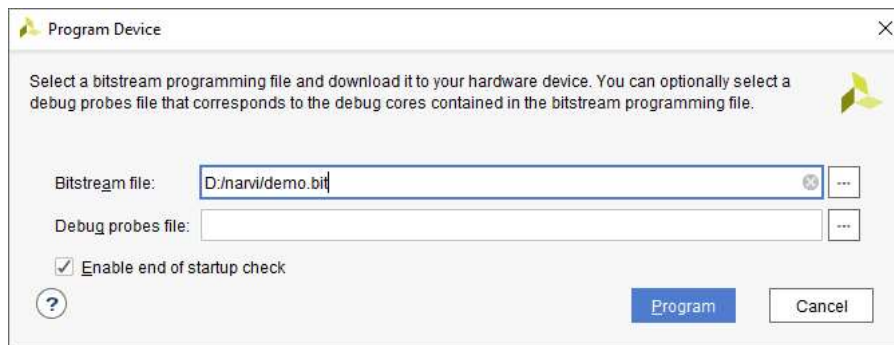
(<https://numato.com/help/wp-content/uploads/2018/05/auto-connect.png>)

Step 3: If the device is detected successfully, then select "Program Device" after right clicking on the target device "xc7s50_0 (1)" as shown below.



(https://numato.com/help/wp-content/uploads/2018/06/narvi_vivado_program_device3.png)

Step 4: In the dialog window which opens up, Vivado automatically chooses correct bitstream file if the design was synthesized, implemented and bitstream generated successfully. If needed, browse to the bitstream which needs to be programmed to FPGA. Finally, click "Program".



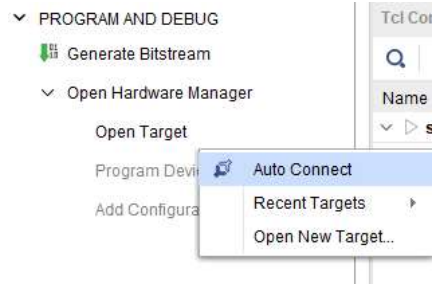
(https://numato.com/help/wp-content/uploads/2018/06/narvi_bit_program.png)

As soon as "Program" is clicked, a green colored DONE LED (D1) on Narvi should light up, indicating that programming process is going on. This LED will turn off when the configuration is complete.

Programming QSPI Flash using Vivado

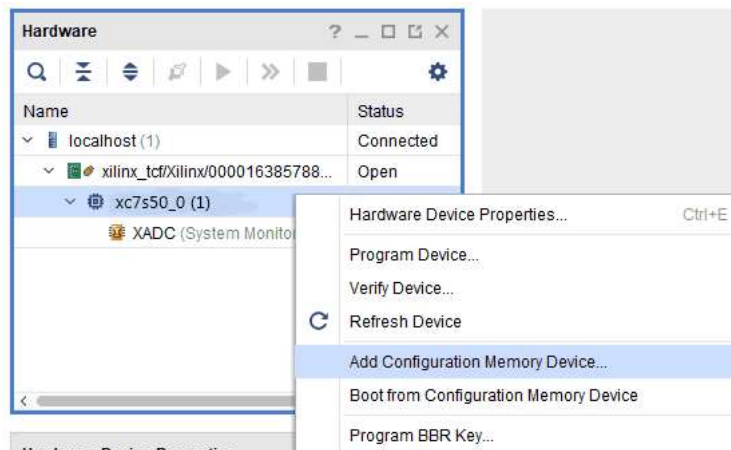
A .bin or .mcs file is required for programming Narvi's onboard QSPI flash.

Step 1: Open Vivado project and open the target by clicking on the "Open Target" in "Open Hardware Manager" in the "Program and Debug" section of the Flow Navigator window. Select "Auto Connect".



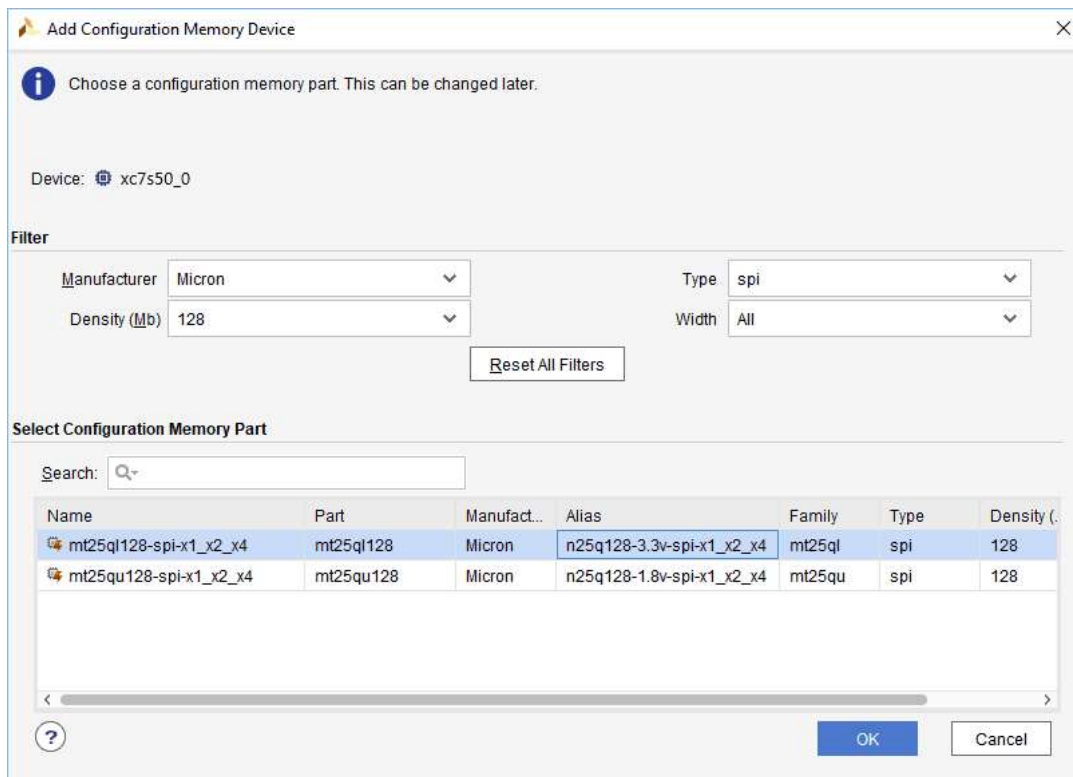
(<https://numato.com/help/wp-content/uploads/2018/05/auto-connect.png>)

Step 2: If the device is detected successfully, then select "Add Configuration Memory Device" after right clicking on the target device "xc7s50_0" as shown below.



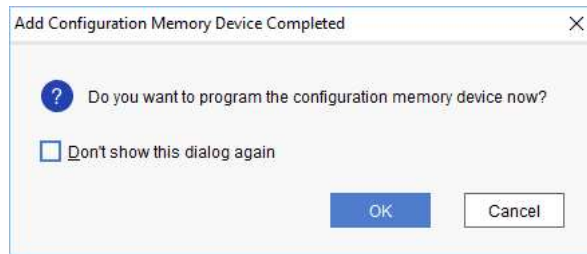
(https://numato.com/help/wp-content/uploads/2018/06/narvi_vivado_add_config_mem.png)

Step 3: Select the memory device "mt25q128-spi-x1_x2_x4 (which is equivalent to n25q128-3.3v-spi-x1_x2_x4)", then click OK.



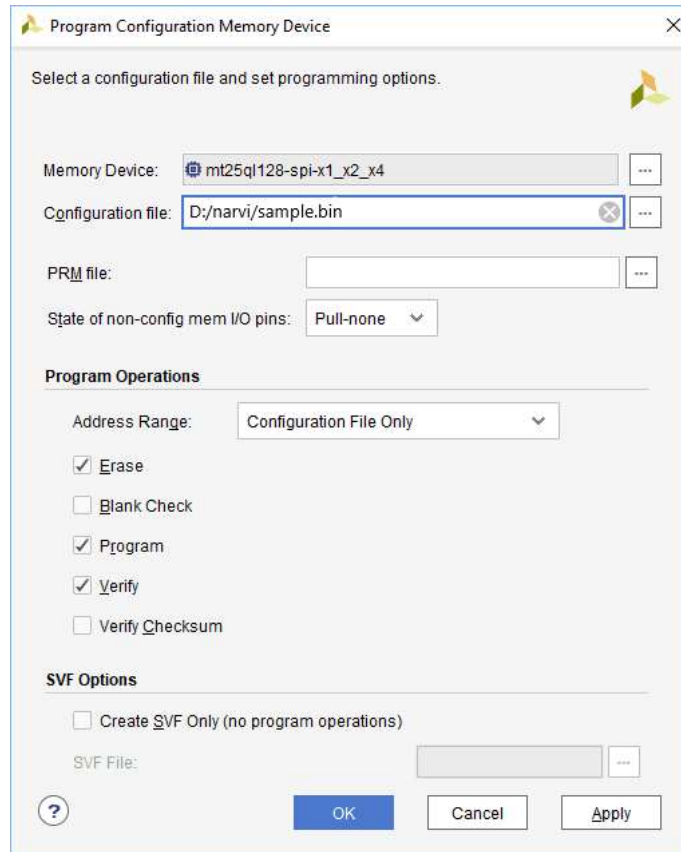
(https://numato.com/help/wp-content/uploads/2018/06/narvi_vivado_select_mem_device1.png)

Step 4: After completion of Step 3 the following dialog box will open. Click OK.



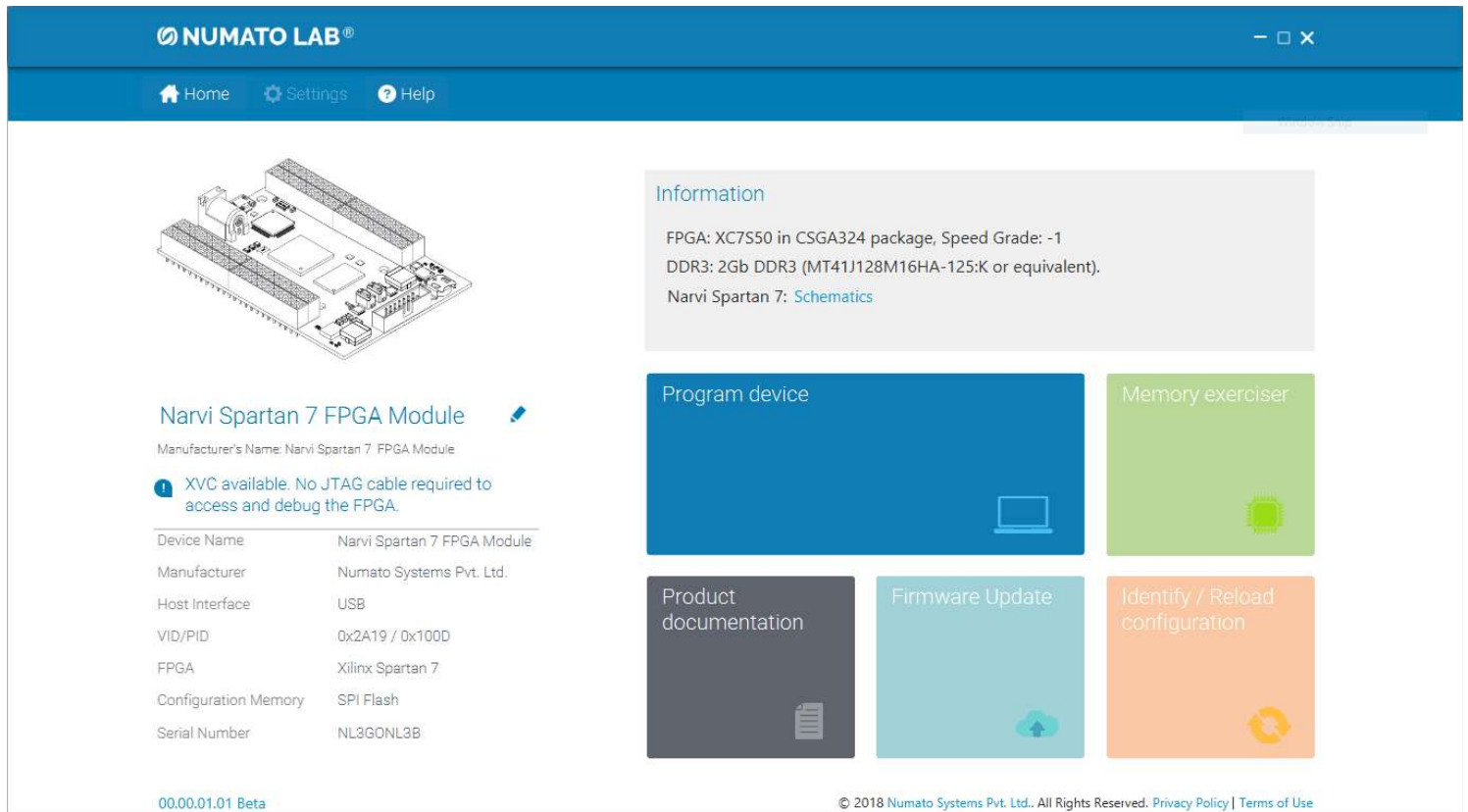
(https://numato.com/help/wp-content/uploads/2018/05/vivado_select_mem_device2.png)

Step 5: Browse to the working .bin file or the .mcs file (whichever applicable) and click OK to program as shown below. If programming is successful, a confirmation message will be displayed.



(https://numato.com/help/wp-content/uploads/2018/06/narvi_prog_config_mem_device.png)

Programming Narvi Using Tenagra



NUMATO LAB®

Home Settings Help

Narvi Spartan 7 FPGA Module

Manufacturer's Name: Narvi Spartan 7 FPGA Module

XVC available. No JTAG cable required to access and debug the FPGA.

Device Name	Narvi Spartan 7 FPGA Module
Manufacturer	Numato Systems Pvt. Ltd.
Host Interface	USB
VID/PID	0x2A19 / 0x100D
FPGA	Xilinx Spartan 7
Configuration Memory	SPI Flash
Serial Number	NL3GONL3B

00.00.01.01 Beta

Information

FPGA: XC7S50 in CSGA324 package, Speed Grade: -1
 DDR3: 2Gb DDR3 (MT41J128M16HA-125:K or equivalent).
 Narvi Spartan 7: [Schematics](#)

Program device

Memory exerciser

Product documentation

Firmware Update

Identify / Reload configuration

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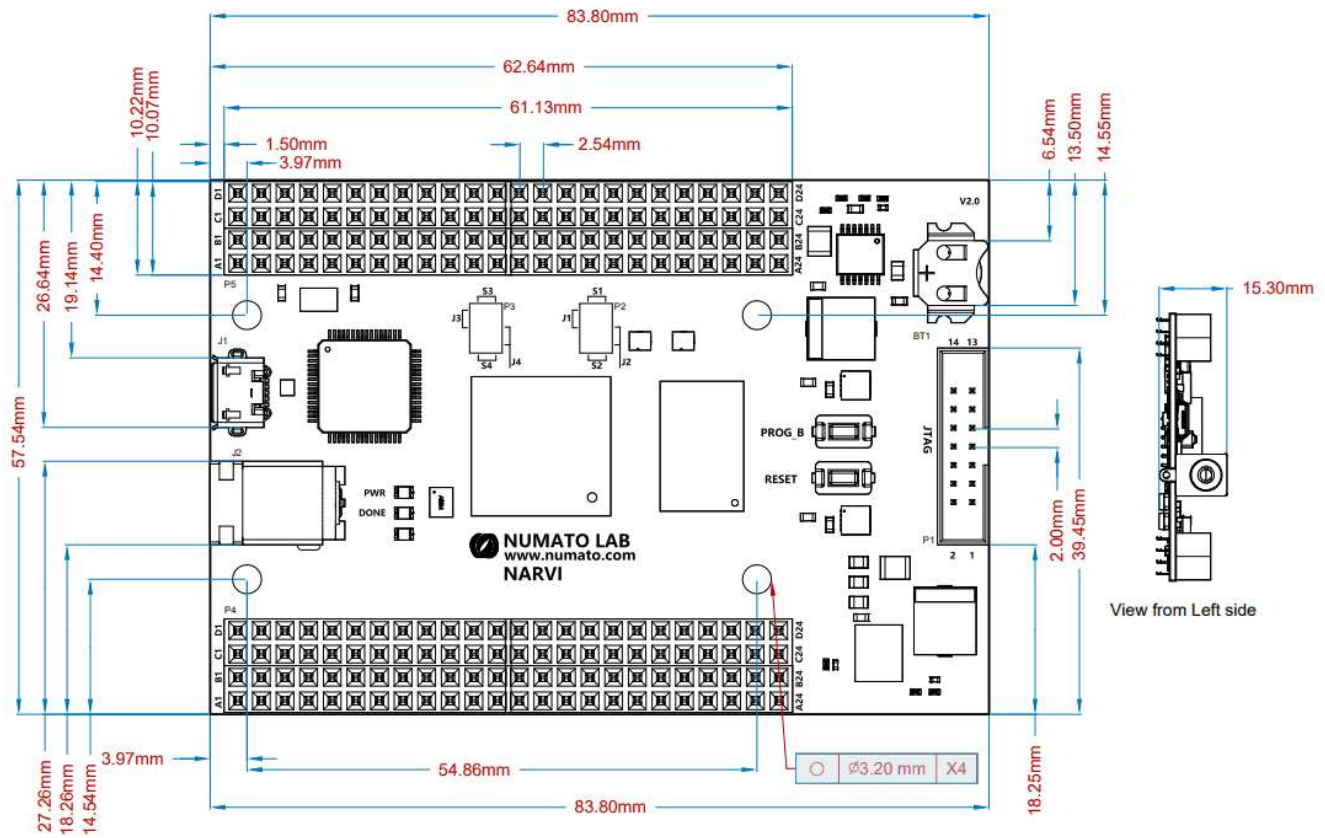
(<https://numato.com/help/wp-content/uploads/2019/02/Narvi-Tenagra.png>)

For steps on how to program Narvi using Tenagra, refer the Getting started with Tenagra FPGA System Management Software (<https://numato.com/kb/getting-started-with-tenagra-fpga-system-management-software/>) article.

Technical Specifications

Parameter *	Value	Unit
Basic Specifications		
Number of GPIOs	130	
On-board oscillator frequency (ASEM1-100.000MHZ-LC-T)	100	MHz
DDR3 SDRAM (MT41J128M16HA - 125 or Equivalent)	2	Gb
Quad SPI Flash Memory (N25Q128A13ESE40E)	128	Mb
Power supply voltage (USB or External)	5 - 12	V
FPGA Specifications		
Internal supply voltage relative to GND	-0.5 to 1.1	V
Auxiliary supply voltage relative to GND	-0.5 to 2.0	V
Output drivers supply voltage relative to GND	-0.5 to 3.6	V

Mechanical Dimensions



(https://numato.com/help/wp-content/uploads/2018/06/Narvi_PD-1.png)

Vivado XDC Constraints

Download XDC Constraints for Vivado (<https://numato.com/download/narvi-constraints-for-vivado/>)

Schematics

Narvi Schematics (<https://numato.com/help/wp-content/uploads/2019/01/NarviSch.pdf>)

Narvi GPIO Trace Length Details

Narvi GPIO Trace Length Details (https://numato.com/help/wp-content/uploads/2019/01/Narvi_GPIO_LengthDetails.pdf)

Narvi GPIO Easy Reference

Narvi GPIO Easy Reference (https://numato.com/help/wp-content/uploads/2018/06/Narvi_GPIO_Easy_Reference1.pdf)

Help Guide Powered by Documentor (https://documentor.in/?utm_source=plugin&utm_medium=footer&utm_campaign=powered-by)