

Product Specification

(Preliminary)

Part Name : OEL Display Module
Customer Part ID :
ZHONGJY Part ID : ZJY-2828TSWAG01
Doc No. : SAS1-0D043-X2

Customer: Approved by

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* This product is only available for China market.

From: ZHONGJY Semiconductor Inc.
Approved by

Notes:

1. Please contact zhongjy Semiconductor Inc. before as signing your product based on this module specification
2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by WiseChip Semiconductor Inc. for any intellectual property claims or other problems that may result from application based on the module described herein.

Revised History

Part Number	Revision	Revision Content	Revised on
ZJY-2828TSWIG01	X1	New	December 9, 2015
ZJY-2828TSWIG01	X2	Page 5 Section 2 - Revised Lifetime Page 6 Section 3.1 - Revised Brightness Page 6 Section 3.2 - Updated DC Characteristics Page 16~19 Section 4.4 - Updated R1 value Page 20 Section 4.5 - Updated Register setting value	January 5, 2016

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1. Basic Specifications

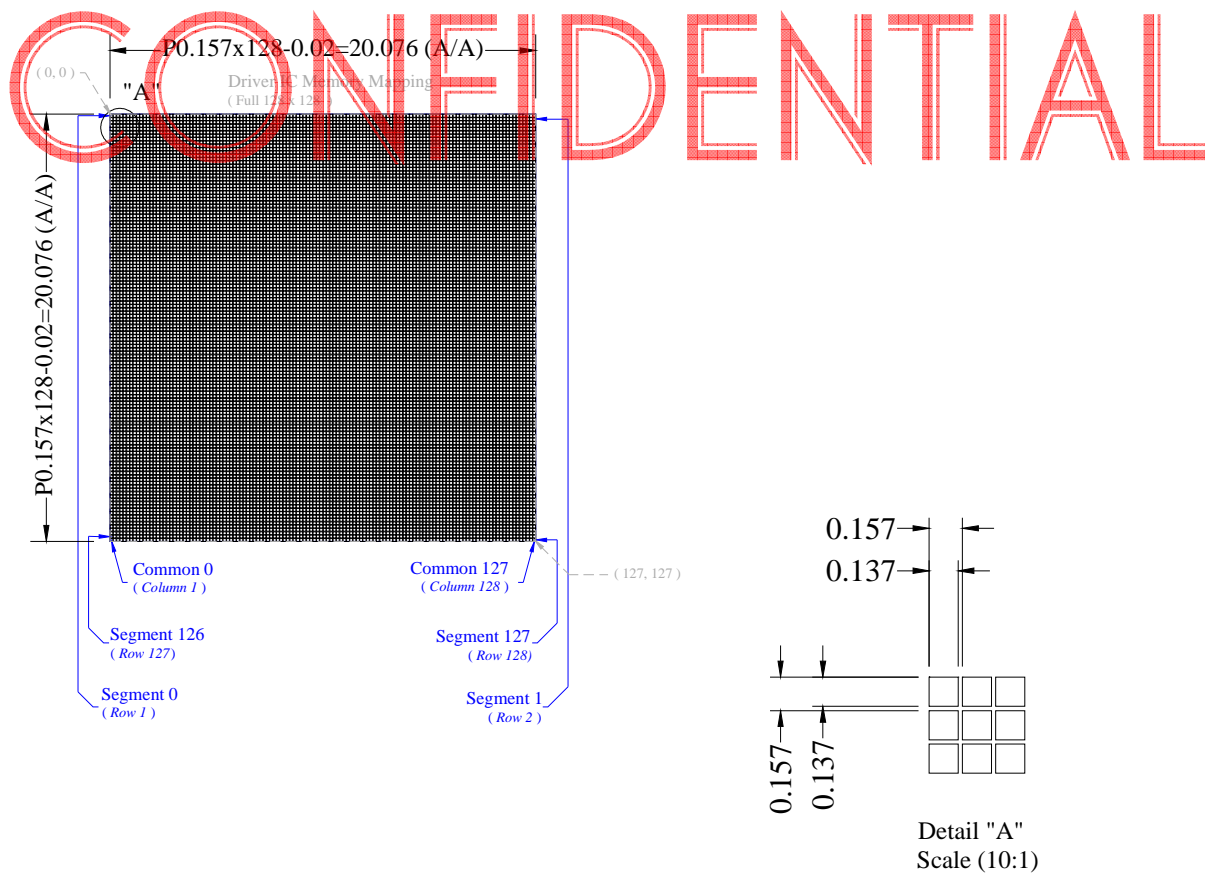
1.1 Display Specifications

- 1) Display Mode : Passive Matrix
- 2) Display Color : Monochrome (White)
- 3) Drive Duty : 1/128 Duty

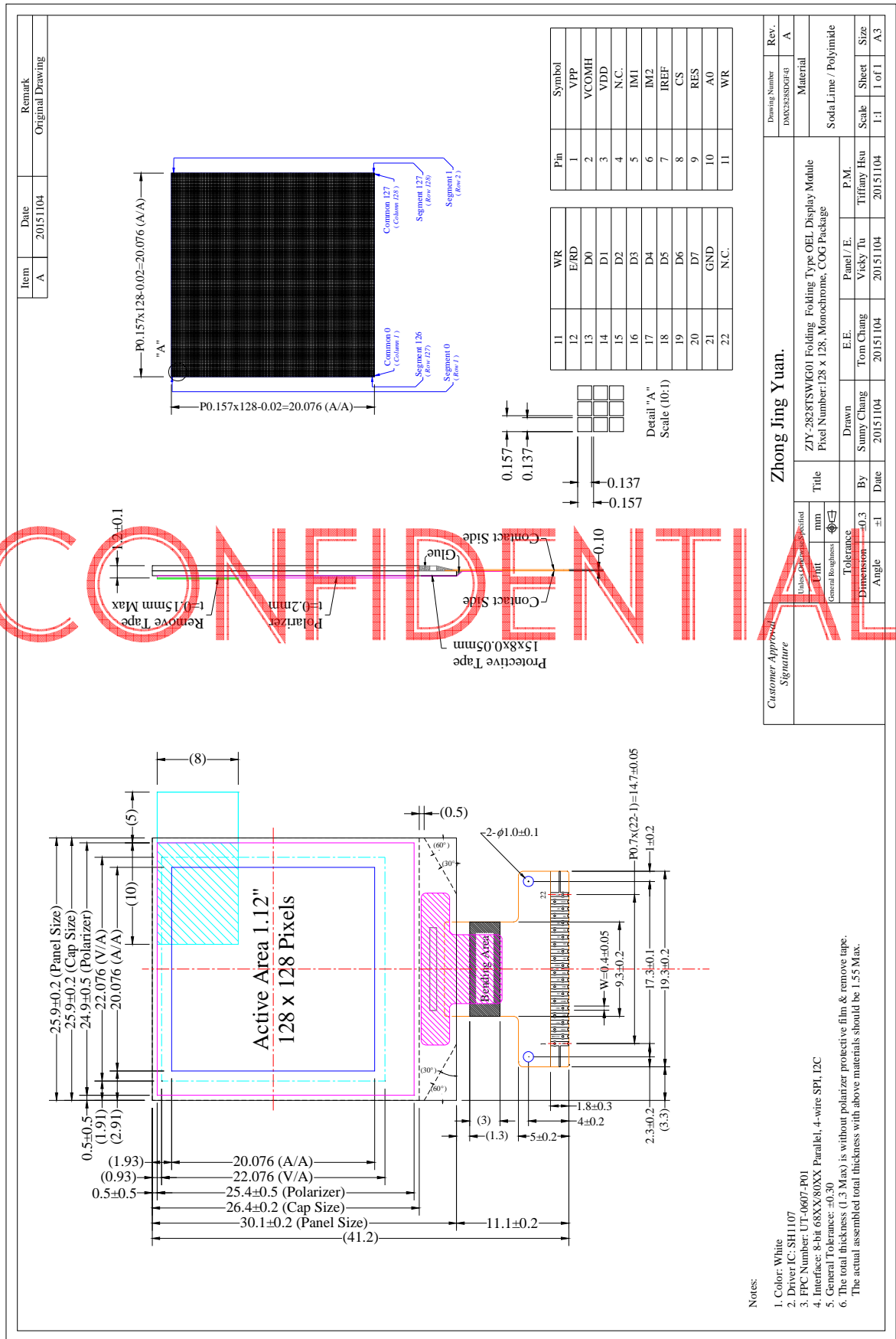
1.2 Mechanical Specifications

- 1) Outline Drawing : According to the annexed outline drawing
- 2) Number of Pixels : 128 × 128
- 3) Module Size : 25.90 × 41.20 × 1.20 (mm)
- 4) Panel Size : 25.90 × 30.10 × 1.20 (mm) including "Anti-Glare Polarizer"
- 5) Active Area : 20.076 × 20.076 (mm)
- 6) Pixel Pitch : 0.157 × 0.157 (mm)
- 7) Pixel Size : 0.137 × 0.137 (mm)
- 8) Weight : T.B.D. (g) ± 10%

1.3 Active Area /Memory Mapping & Pixel Construction



1.4 Mechanical Drawing



The drawing contained herein is the exclusive property of WiseChip. It is not allowed to copy, reproduce and or disclose in any formats without permission of WiseChip.

1.5 Pin Definition

Pin Number	Symbol	I/O	Function															
Power Supply																		
1	VPP	P	Power Supply for OEL Panel This is the most positive voltage supply pin of the chip. It must be supplied externally.															
3	VDD	P	Power Supply for Logic This is a voltage supply pin. It must be connected to external source.															
21	GND	P	Ground of OEL System This is a ground pin. It also acts as a reference for the logic pins, the OEL driving voltages, and the analog circuits. It must be connected to external ground.															
Driver																		
2	VCOMH	O	Voltage Output High Level for COM Signal This pin is for the voltage output high level for COM signals. A capacitor should be connected between this pin and GND.															
7	IREF	O	Current Reference for Brightness Adjustment This pin is segment current reference pin. A resistor should be connected between this pin and GND. Set the current at 15.625 μ A maximum.															
Interface																		
5 6	IM1 IM2	I	<p>Communicating Protocol Select These pins are MCU interface selection input. See the following table:</p> <table border="1"> <thead> <tr> <th></th> <th>IM2</th> <th>IM1</th> </tr> </thead> <tbody> <tr> <td>4-wire SPI</td> <td>0</td> <td>0</td> </tr> <tr> <td>I²C</td> <td>0</td> <td>1</td> </tr> <tr> <td>8-bit 68XX Parallel</td> <td>1</td> <td>0</td> </tr> <tr> <td>8-bit 80XX Parallel</td> <td>1</td> <td>1</td> </tr> </tbody> </table>		IM2	IM1	4-wire SPI	0	0	I ² C	0	1	8-bit 68XX Parallel	1	0	8-bit 80XX Parallel	1	1
	IM2	IM1																
4-wire SPI	0	0																
I ² C	0	1																
8-bit 68XX Parallel	1	0																
8-bit 80XX Parallel	1	1																
8	CS	I	Chip Select This pin is the chip select input. The chip is enabled for MCU communication only when CSB is pulled low.															
9	RES	I	Power Reset for Controller and Driver This pin is reset signal input. When the pin is low, initialization of the chip is executed.															
10	A0	I	Data/Command Control This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 will be interpreted as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. When the pin is pulled high and serial interface mode is selected, the data at SI will be interpreted as data. When it is pulled low, the data at SI will be transferred to the command register. In I ² C mode, this pin acts as SA0 for slave address selection. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.															
11	WR	I	Read/Write Select or Write This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it to "Low" for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low. When serial or I ² C mode is selected, this pin must be connected to V _{DD} .															
12	E/RD	I	Read/Write Enable or Read This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low. When serial or I ² C mode is selected, this pin must be connected to V _{DD} .															
13~20	D0~D7	I/O	Host Data Input/Output Bus These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SI and D0 will be the serial clock input SCL. When I ² C mode is selected, D1 be the serial data input SDA and D0 is the serial clock input, SCL. Unused pins(D2~D7) must be set to high impedance.															

1.5 Pin Definition (Continued)

Pin Number	Symbol	I/O	Function
<i>Reserve</i>			
4, 22	N.C.	-	Reserved Pin The N.C. pins between function pins are reserved for compatible and flexible design.

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2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	V _{DD}	-0.3	3.6	V	1, 2
Supply Voltage for Display	V _{PP}	0	16	V	1, 2
Operating Temperature	T _{OP}	-40	70	°C	
Storage Temperature	T _{STG}	-40	85	°C	3
Life Time (120 cd/m ²)		10,000	-	hour	4

Note 1: All the above voltages are on the basis of "GND = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: End of lifetime is specified as 50% of initial brightness reached. The reference average operation life time at room temperature is estimated by the accelerated at high temperature conditions.

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3. Optics & Electrical Characteristics

3.1 Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	L_{br}	Note 4	100	120	-	cd/m ²
C.I.E. (White)	(x)	C.I.E. 1931	0.25	0.29	0.33	
	(y)		0.27	0.31	0.35	
Dark Room Contrast	CR		-	>10,000:1	-	
Viewing Angle			-	Free	-	degree

* Optical measurement taken at $V_{DD} = 3.0V$, $V_{PP} = 13.5V$.
Software configuration follows Section 4.5 Initialization.

3.2 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	V_{DD}		1.65	3.0	3.5	V
Supply Voltage for Display	V_{PP}	Note 5	13	13.5	14	V
High Level Input	V_{IHC}		$0.8 \times V_{DD}$	-	V_{DD}	V
Low Level Input	V_{ILC}		0	-	$0.2 \times V_{DD}$	V
High Level Output	V_{OHC}	$I_{OH} = -500\mu A$	$0.8 \times V_{DD}$	-	V_{DD}	V
Low Level Output	V_{OLC}	$I_{OL} = 500\mu A$	0	-	$0.2 \times V_{DD}$	V
Operating Current for V_{DD}	I_{DD}		-	110	160	μA
Operating Current for V_{PP}	I_{PP}	Note 6	-	9.2	11.5	mA
		Note 7	-	14.8	18.5	mA
		Note 8	-	28.9	36.1	mA
Sleep Mode Current for V_{DD}	$I_{DD, SLEEP}$		-	-	5	μA
Sleep Mode Current for V_{PP}	$I_{PP, SLEEP}$		-	-	5	μA

Note 5: Brightness (L_{br}) and Supply Voltage for Display (V_{PP}) are subject to the change of the panel characteristics and the customer's request.

Note 6: $V_{DD} = 3.0V$, $V_{PP} = 13.5V$, 30% Display Area Turn on.

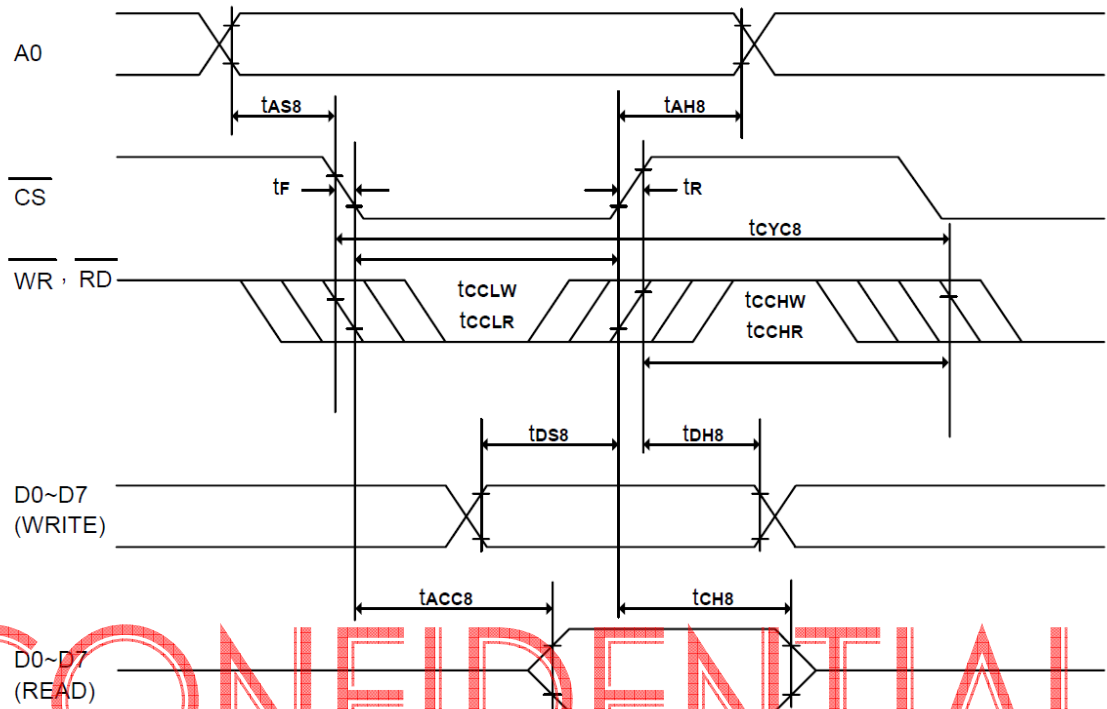
Note 7: $V_{DD} = 3.0V$, $V_{PP} = 13.5V$, 50% Display Area Turn on.

Note 8: $V_{DD} = 3.0V$, $V_{PP} = 13.5V$, 100% Display Area Turn on.

* Software configuration follows Section 4.5 Initialization.

3.3 AC Characteristics

3.3.1 8080 Series MPU interface Timing Characteristics:



($V_{DD} - GND = 1.65\text{V to } 2.4\text{V}$, $T_a = 25^\circ\text{C}$)

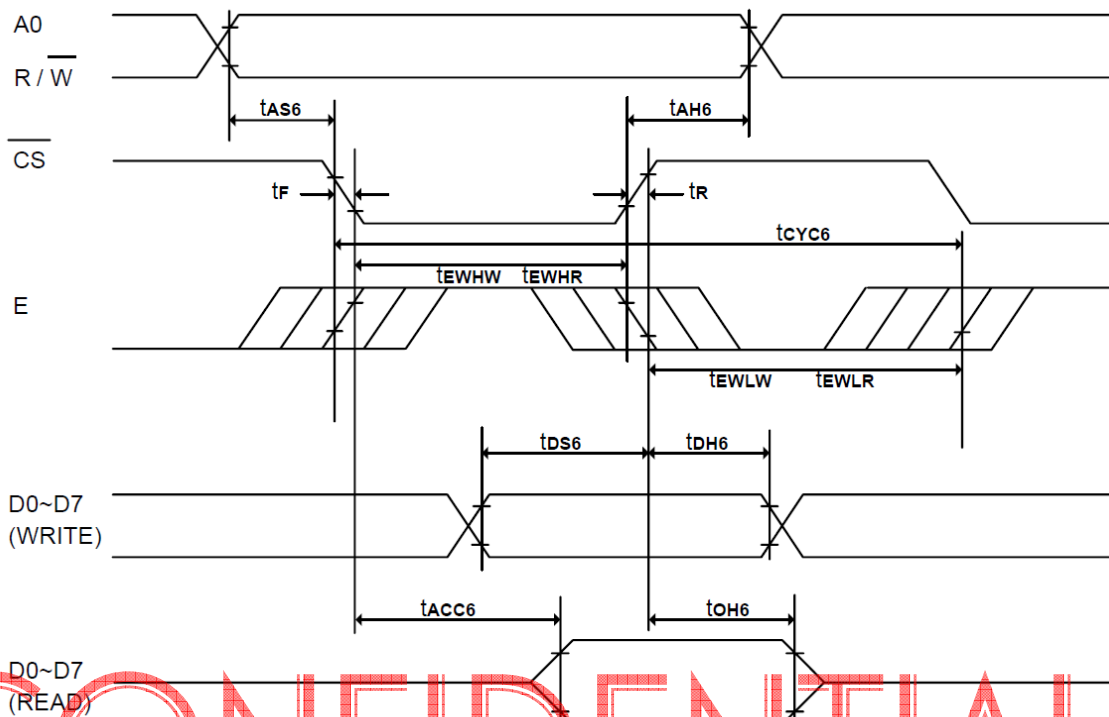
Symbol	Description	Min	Max	Unit
t_{CYC8}	System Clock Cycle Time	300		ns
t_{AS8}	Address Setup Time	0		ns
t_{AH8}	Address Hold Time	0		ns
t_{DS8}	Data Setup Time	40		ns
t_{DH8}	Data Hold Time	30		ns
t_{CH8}	Output disable Time ($C_L = 100\text{pF}$)	10	70	ns
t_{ACC8}	RD access Time ($C_L = 100\text{pF}$)	-	280	ns
t_{CCLW}	WR control L pulse width	100		ns
t_{CCLR}	RD control L pulse width	120		ns
t_{CCHW}	WR control H pulse width	100		ns
t_{CCHR}	RD control H pulse width	100		ns
t_R	Rise Time		15	ns
t_F	Fall Time		15	ns

($V_{DD} - GND = 2.4V$ to $3.5V$, $T_a = 25^{\circ}C$)

Symbol	Description	Min	Max	Unit
t_{CYC8}	System Clock Cycle Time	300		ns
t_{AS8}	Address Setup Time	0		ns
t_{AH8}	Address Hold Time	0		ns
t_{DS8}	Data Setup Time	40		ns
t_{DH8}	Data Hold Time	15		ns
t_{CH8}	Output disable Time ($C_L = 100pF$)	10	70	ns
t_{ACC8}	RD access Time ($C_L = 100pF$)	-	140	ns
t_{CCLW}	WR control L pulse width	100		ns
t_{CCLR}	RD control L pulse width	120		ns
t_{CCHW}	WR control H pulse width	100		ns
t_{CCHR}	RD control H pulse width	100		ns
t_R	Rise Time		15	ns
t_F	Fall Time		15	ns

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3.3.2 6800 Series MPU interface Timing Characteristics:



($V_{DD} - GND = 1.65V$ to $2.4V$, $T_a = 25^\circ C$)

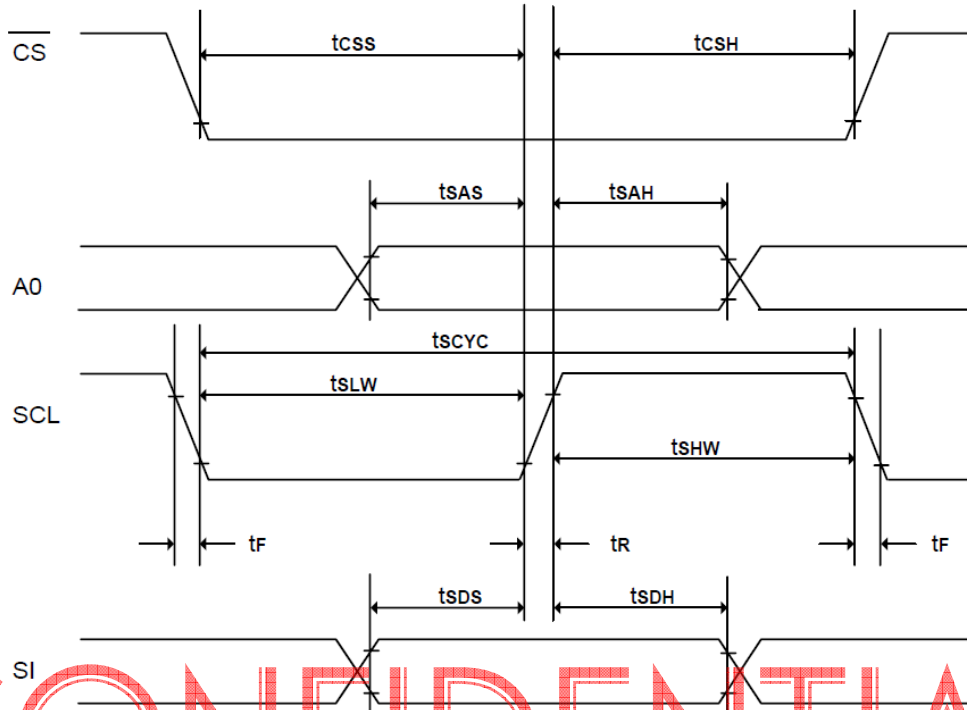
Symbol	Description	Min	Max	Unit
t_{CYC6}	System Clock Cycle Time	300		ns
t_{AS6}	Address Setup Time	0		ns
t_{AH6}	Address Hold Time	0		ns
t_{DS6}	Data Setup Time	40		ns
t_{DH6}	Data Hold Time	30		ns
t_{OH6}	Output disable Time	10	70	ns
t_{ACC6}	RD access Time	-	280	ns
t_{EWHW}	Enable control H pulse width(Write)	100		ns
t_{EWHR}	Enable control H pulse width(Read)	120		ns
t_{EWLW}	Enable control L pulse width(Write)	100		ns
t_{EWLR}	Enable control L pulse width(Read)	100		ns
t_R	Rise Time		15	ns
t_F	Fall Time		15	ns

($V_{DD} - GND = 2.4V$ to $3.5V$, $T_a = 25^{\circ}C$)

Symbol	Description	Min	Max	Unit
t_{CYC6}	System Clock Cycle Time	300		ns
t_{AS6}	Address Setup Time	0		ns
t_{AH6}	Address Hold Time	0		ns
t_{DS6}	Data Setup Time	40		ns
t_{DH6}	Data Hold Time	15		ns
t_{OH6}	Output disable Time ($C_L = 100pF$)	10	70	ns
t_{ACC6}	RD access Time ($C_L = 100pF$)	-	140	ns
t_{EWHW}	Enable control H pulse width(Write)	100		ns
t_{EWHR}	Enable control H pulse width(Read)	120		ns
t_{EWLW}	Enable control L pulse width(Write)	100		ns
t_{EWLR}	Enable control L pulse width(Read)	100		ns
t_R	Rise Time		15	ns
t_F	Fall Time		15	ns

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3.3.3 4-wire SPI interface Timing Characteristics:



($V_{DD} - GND = 1.65V$ to $2.4V$, $T_a = 25^\circ C$)

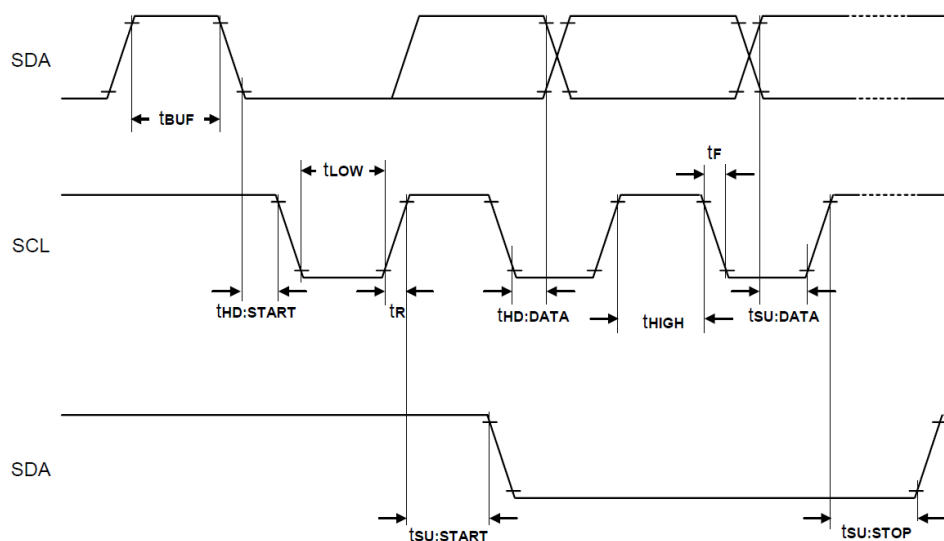
Symbol	Description	Min	Max	Unit
t_{SCYC}	Serial Clock Cycle Time	500	-	ns
t_{SAS}	Address Setup Time	300	-	ns
t_{SAH}	Address Hold Time	300	-	ns
t_{SDS}	Data Setup Time	200	-	ns
t_{SDH}	Data Hold Time	200	-	ns
t_{CSS}	Chip Select Setup Time	240	-	ns
t_{CSH}	Chip Select Hold Time	120	-	ns
t_{SHW}	Serial Clock H Pulse Width	200	-	ns
t_{SLW}	Serial Clock L Pulse Width	200	-	ns
t_R	Rise Time	-	30	ns
t_F	Fall Time	-	30	ns

($V_{DD} - GND = 2.4V$ to $3.5V$, $T_a = 25^\circ C$)

Symbol	Description	Min	Max	Unit
t_{SCYC}	Serial Clock Cycle Time	250	-	ns
t_{SAS}	Address Setup Time	150	-	ns
t_{SAH}	Address Hold Time	150	-	ns
t_{SDS}	Data Setup Time	100	-	ns
t_{SDH}	Data Hold Time	100	-	ns
t_{CSS}	Chip Select Setup Time	120	-	ns
t_{CSH}	Chip Select Hold Time	60	-	ns
t_{SHW}	Serial Clock H Pulse Width	100	-	ns
t_{SLW}	Serial Clock L Pulse Width	100	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

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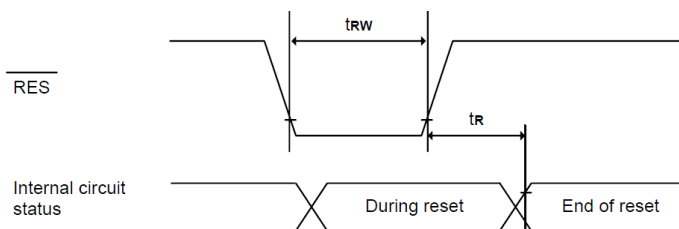
3.3.4 I2C interface Timing Characteristics:



($V_{DD} - GND = 1.65V$ to $3.5V$, $T_a = 25^\circ C$)

Symbol	Description	Min	Max	Unit
f_{SCL}	SCL Clock frequency	DC	400	KHz
t_{LOW}	SCL clock Low pulse width	1.3	-	μS
t_{HIGH}	SCL clock High pulse width	0.6	-	μS
$t_{SU:DATA}$	Data Setup Time	100	-	ns
$t_{HD:DATA}$	Data Hold Time	0	0.9	μS
t_R	SCL, SDA Rise Time	$20+0.1C_b$	300	ns
t_F	SCL, SDA Fall Time	$20+0.1C_b$	300	ns
C_b	Capacity load on each bus line		400	pF
$t_{SU:START}$	Setup Time for re-START	0.6	-	μS
$t_{HD:START}$	START Hold Time	0.6	-	μS
$t_{HD:STOP}$	Setup Time for STOP	0.6	-	μS
t_{BUF}	Bus free times between STOP and START condition	1.3	-	μS

3.3.5 Reset Timing Characteristics:



($V_{DD} - GND = 1.65V$ to $3.5V$, $T_a = 25^\circ C$)

Symbol	Description	Min	Max	Unit
t_R	Reset time	-	2.0	μS
t_{RW}	Reset Low pulse width	10.0	-	μS

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4. Functional Specification

4.1 Commands

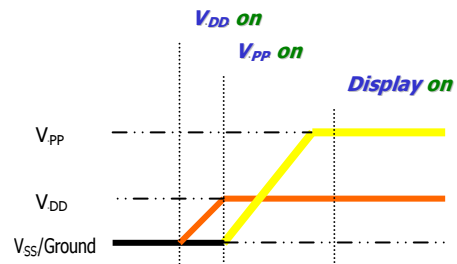
Refer to the Technical Manual for the SH1107

4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

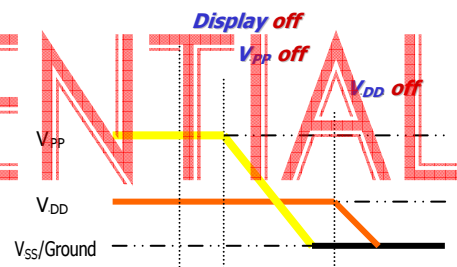
4.2.1 Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{PP}
6. Delay 100ms
(When V_{PP} is stable)
7. Send Display on command



4.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{PP}
3. Delay 100ms
(When V_{PP} is reach 0 and panel is completely discharges)
4. Power down V_{DD}



Note 9:

- 1) Since an ESD protection circuit is connected between V_{DD} and V_{PP} inside the driver IC, V_{PP} becomes lower than V_{DD} whenever V_{DD} is ON and V_{PP} is OFF.
- 2) V_{PP} should be kept float (disable) when it is OFF.
- 3) Power Pins (V_{DD} , V_{PP}) can never be pulled to ground under any circumstance.
- 4) V_{DD} should not be power down before V_{PP} power down.

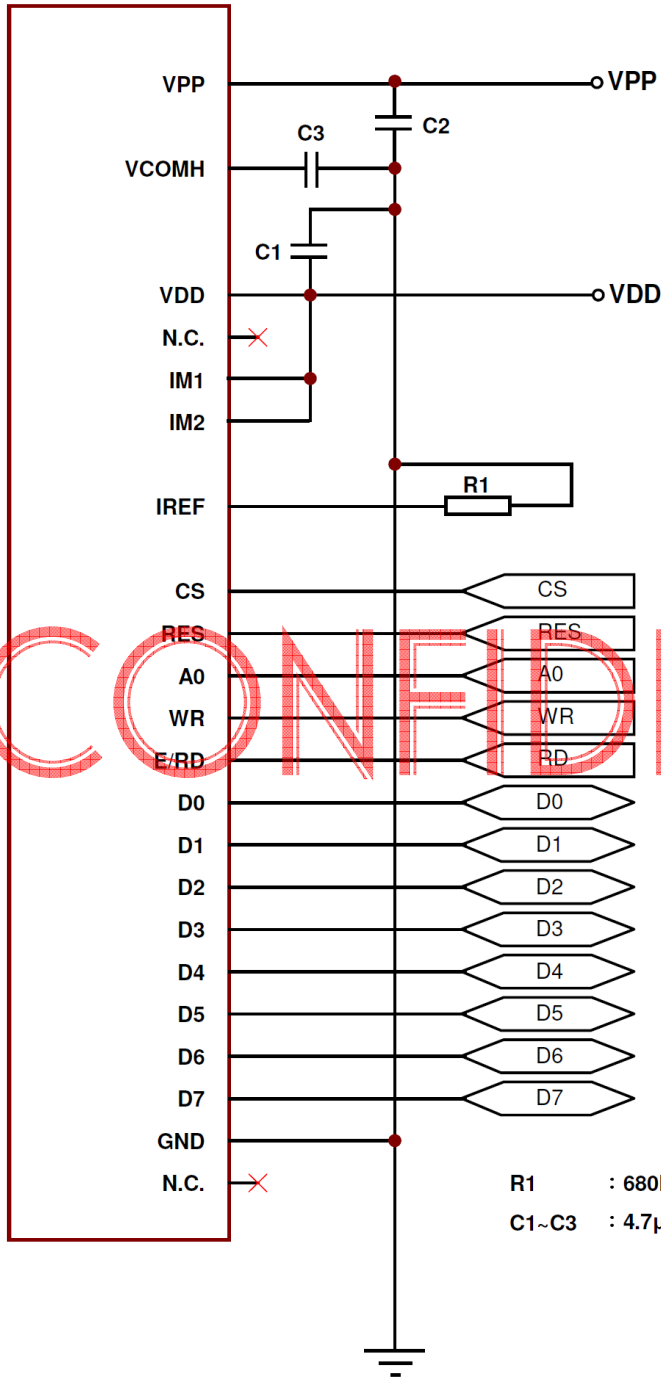
4.3 Reset Circuit

When RESB input is low, the chip is initialized with the following status:

1. Display is OFF. Common and Segment are in high impedance state.
2. 128×128 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 is mapped to the top line of the display).
4. Shift register data clear in serial interface
5. Column address counter is set at 0
6. Normal scan direction of the COM outputs
7. Contrast control register is set at 80h
8. Internal DC-DC is selected

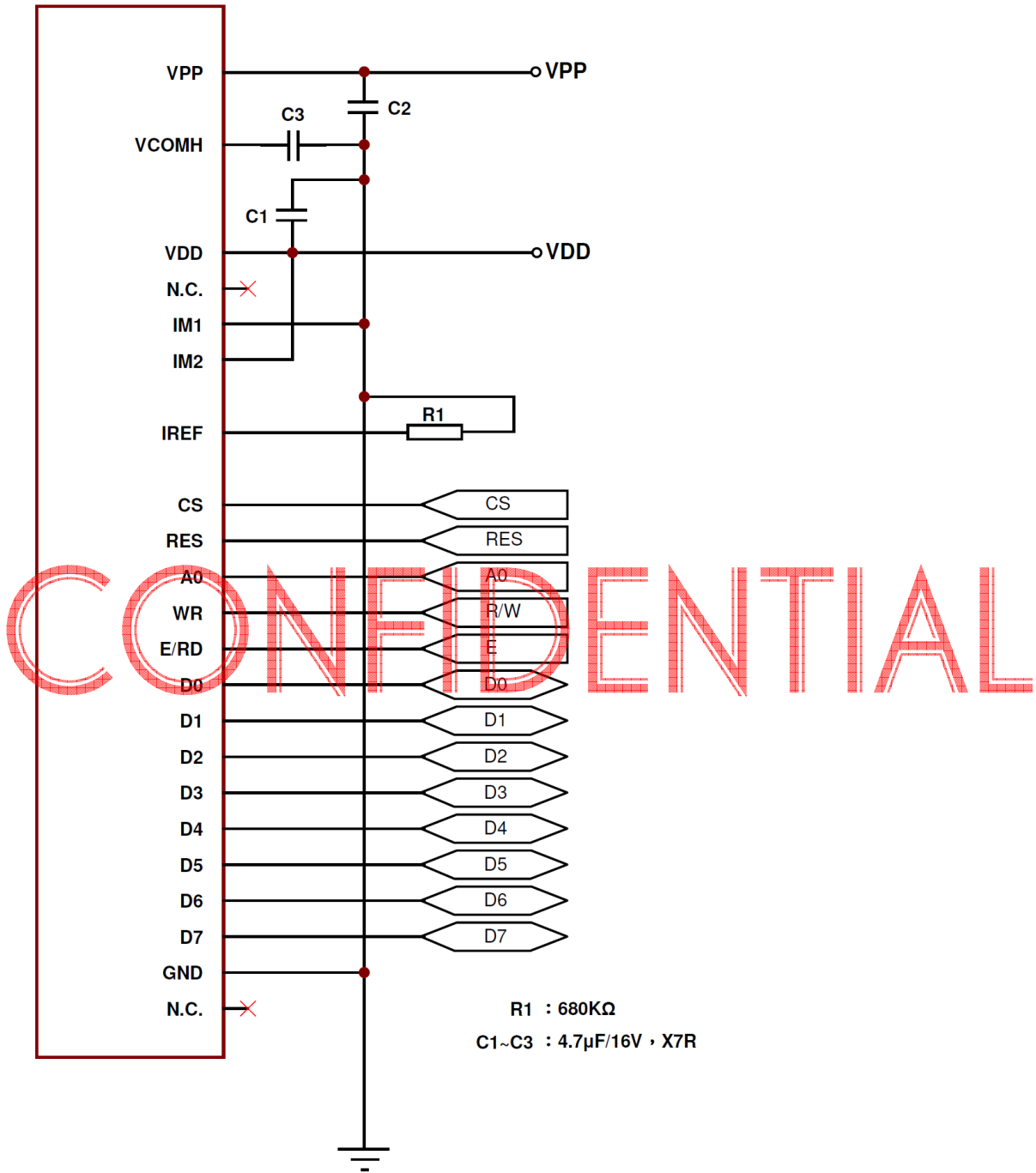
4.4 Application Circuit

4.4.1 8080 Series MPU interface

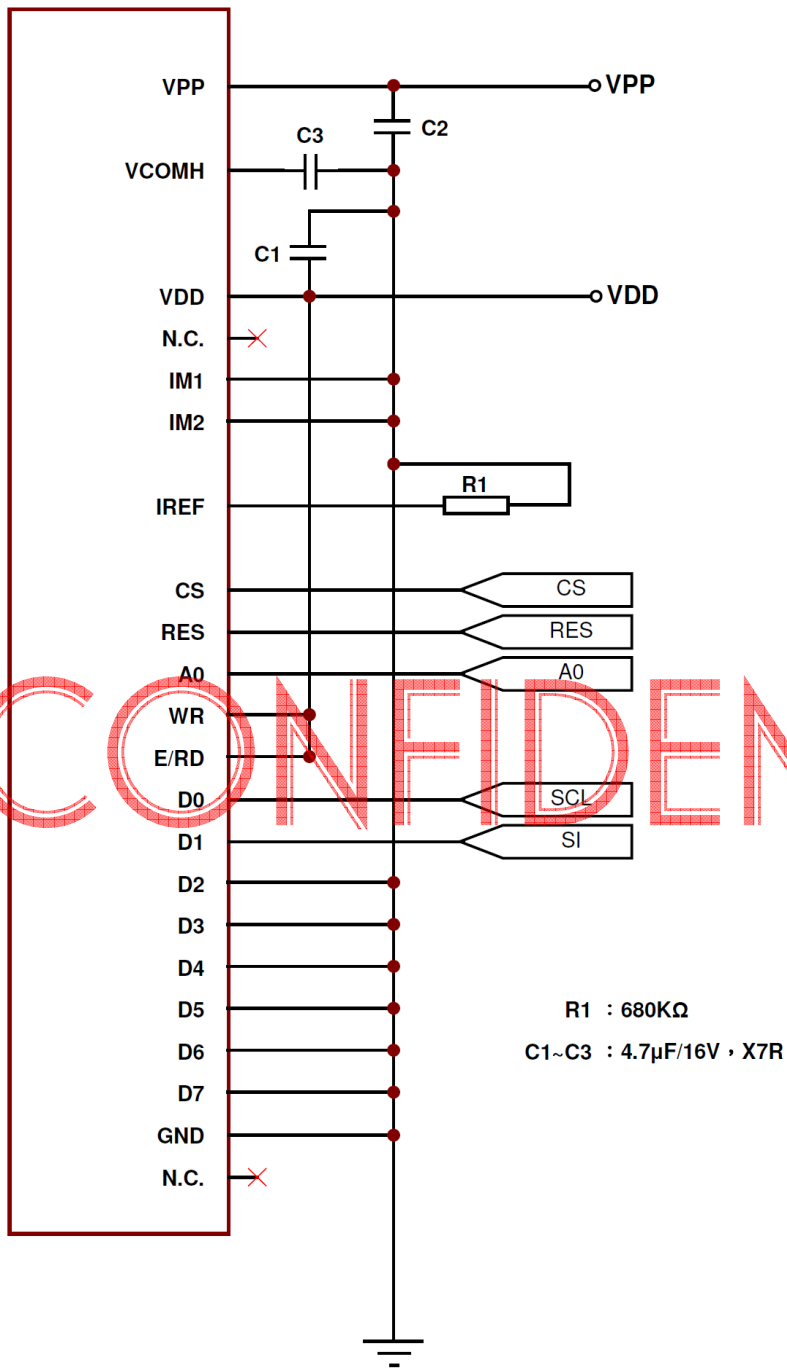


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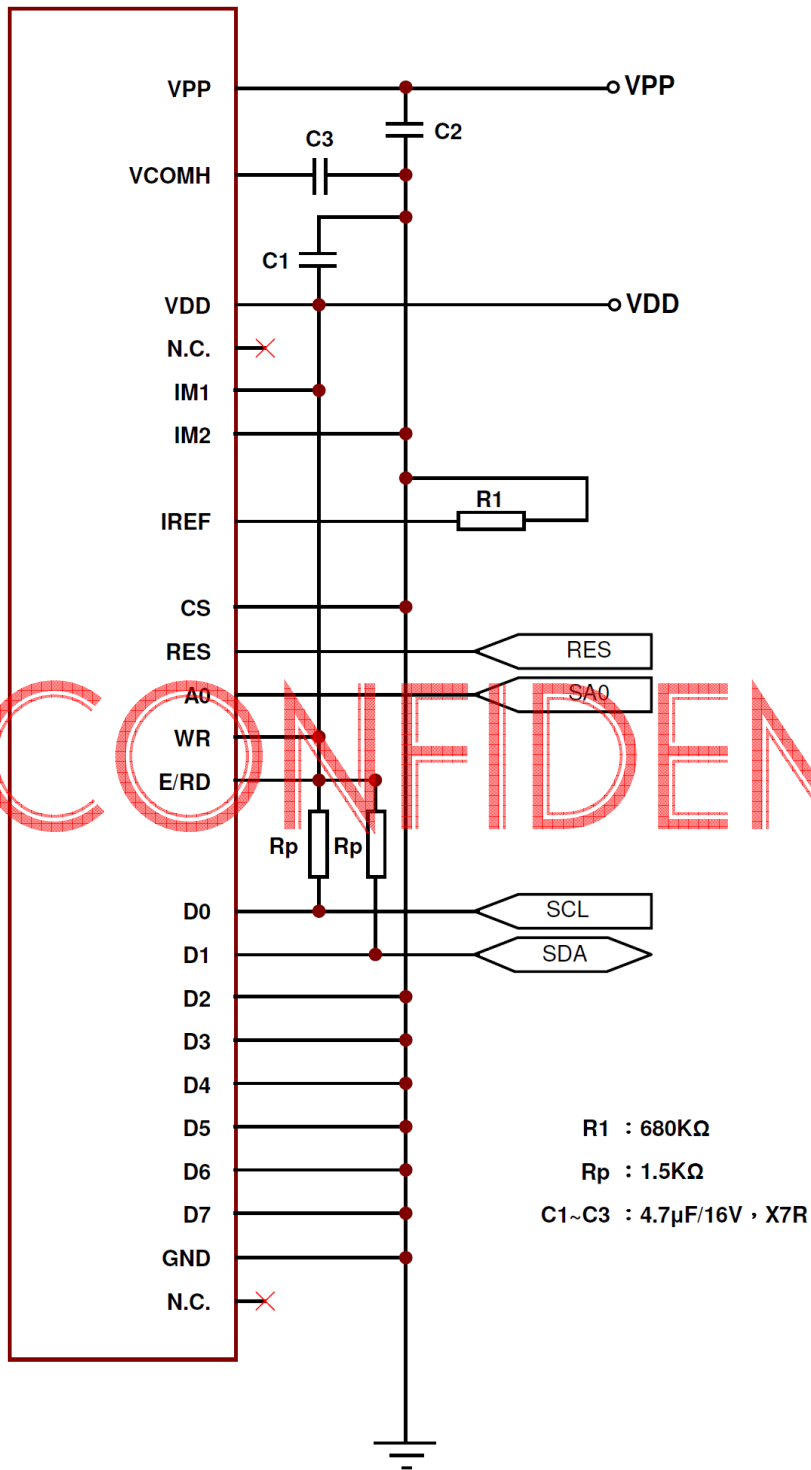
4.4.2 6800 Series MPU interface



4.4.3 4-wire SPI interface



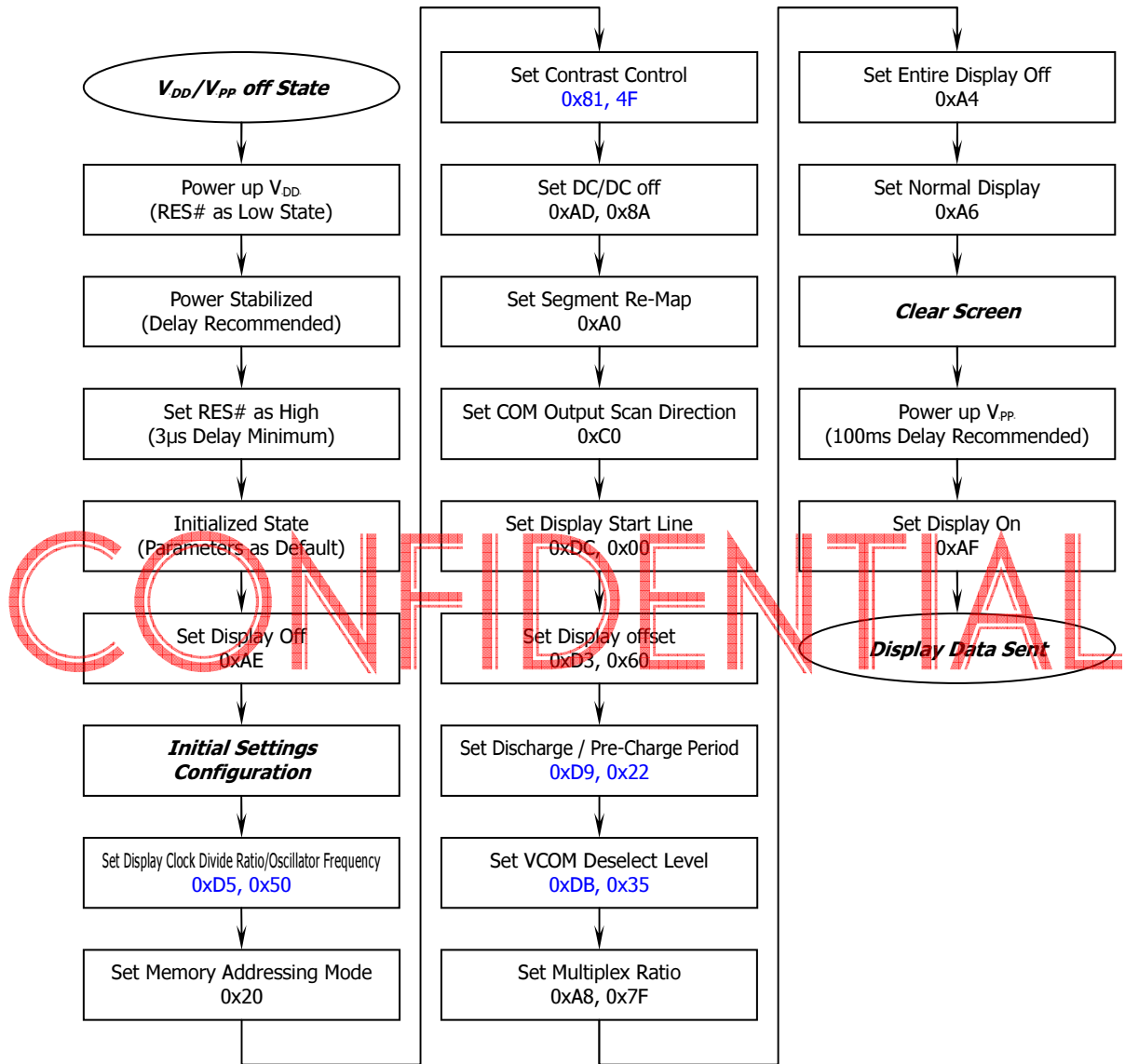
4.4.4 I²C interface



4.5 Actual Application Example

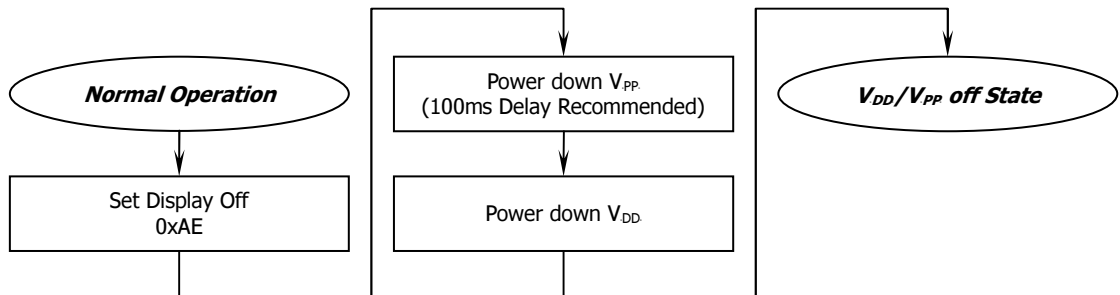
Command usage and explanation of an actual example

<Power up Sequence>

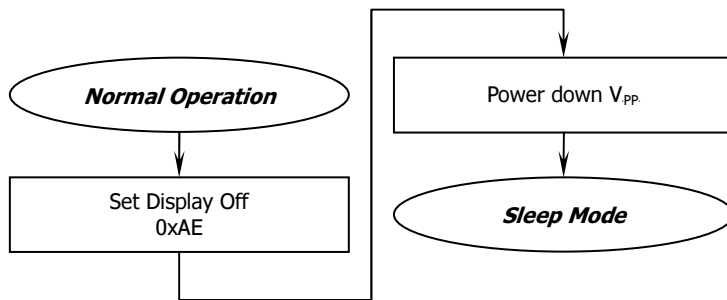


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

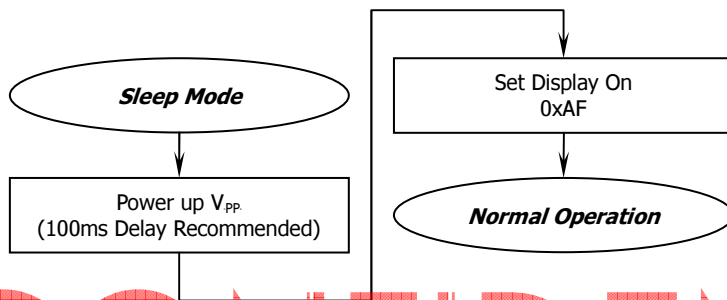
<Power down Sequence>



<Entering Sleep Mode>



<Exiting Sleep Mode>



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5. Reliability

5.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	70°C, 240 hrs	The operational functions work.
Low Temperature Operation	-40°C, 240 hrs	
High Temperature Storage	85°C, 240 hrs	
Low Temperature Storage	-40°C, 240 hrs	
High Temperature/Humidity Operation	60°C, 90% RH, 120 hrs	
Thermal Shock	-40°C ↔ 85°C, 24 cycles 60 mins dwell	

* The samples used for the above tests do not include polarizer.

* No moisture condensation is observed during tests.

5.2 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

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6. Outgoing Quality Control Specifications

6.1 Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature:	23 ± 5°C
Humidity:	55 ± 15% RH
Fluorescent Lamp:	30W
Distance between the Panel & Lamp:	≥ 50cm
Distance between the Panel & Eyes of the Inspector:	≥ 30cm
Finger glove (or finger cover) must be worn by the inspector.	
Inspection table or jig must be anti-electrostatic.	

6.2 Sampling Plan

Level II, Normal Inspection, Single Sampling, MIL-STD-105E

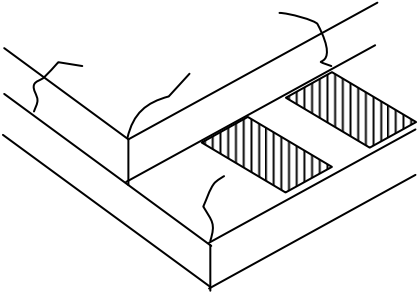

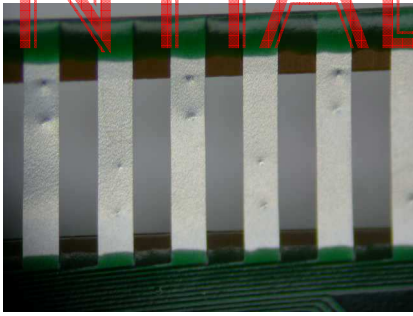
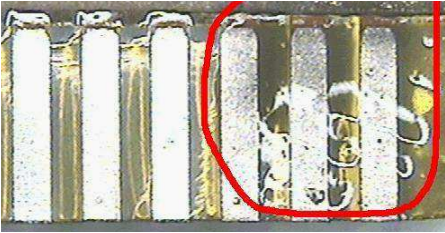
6.3 Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

6.3.1 Cosmetic Check (Display Off) in Non-Active Area

Check Item	Classification	Criteria
Panel General Chipping	Minor	<p>X > 6 mm (Along with Edge) Y > 1 mm (Perpendicular to edge)</p>

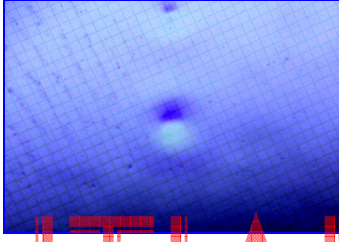
6.3.1 Cosmetic Check (Display Off) in Non-Active Area (Continued)

Check Item	Classification	Criteria
Panel Crack	Minor	Any crack is not allowable. 
Copper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Terminal Lead Prober Mark	Acceptable	
Glue or Contamination on Pin (Couldn't Be Removed by Alcohol)	Minor	
Ink Marking on Back Side of panel (Exclude on Film)	Acceptable	Ignore for Any

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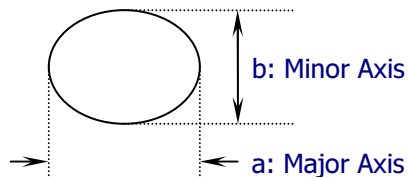
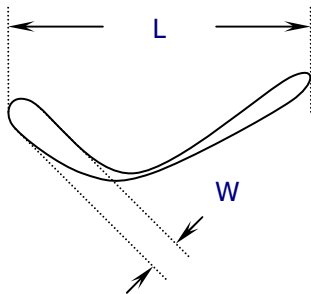
6.3.2 Cosmetic Check (Display Off) in Active Area

It is recommended to execute in clear room environment (class 10k) if actual in necessary.

Check Item	Classification	Criteria
Any Dirt & Scratch on Protective Film	Acceptable	Ignore for Any
Scratches, Fiber, Line-Shape Defect (On Polarizer)	Minor	$W \leq 0.1$ Ignore $W > 0.1$ $L \leq 2$ $n \leq 1$ $L > 2$ $n = 0$
Dirt, Spot-Shape Defect (On Polarizer)	Minor	$\Phi \leq 0.1$ Ignore $0.1 < \Phi \leq 0.25$ $n \leq 1$ $0.25 < \Phi$ $n = 0$
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	$\Phi \leq 0.5$ → Ignore if no Influence on Display $0.5 < \Phi$ $n = 0$ 
Fingerprint, Flow Mark (On Polarizer)	Minor	Not Allowable

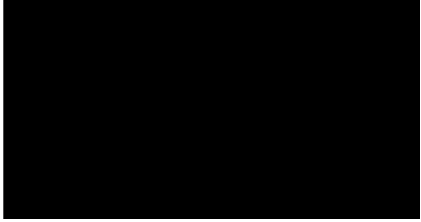
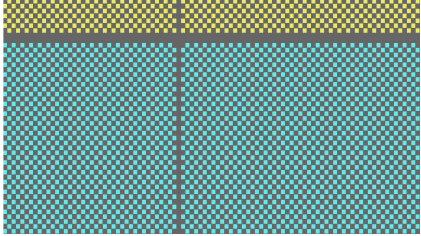
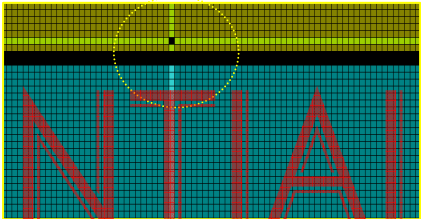
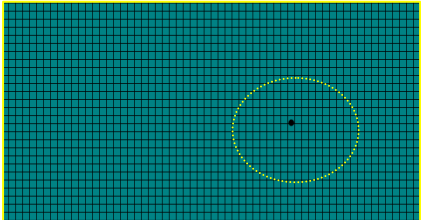
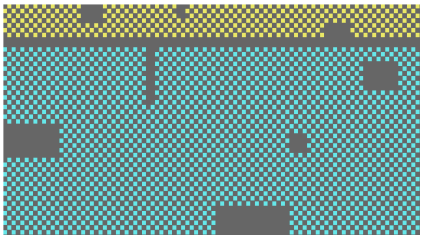
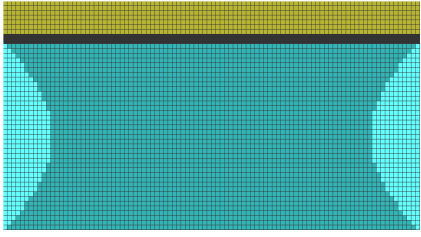
* Protective film should not be tear off when cosmetic check.

* Definition of W & L & Φ (Unit: mm): $\Phi = (a + b) / 2$



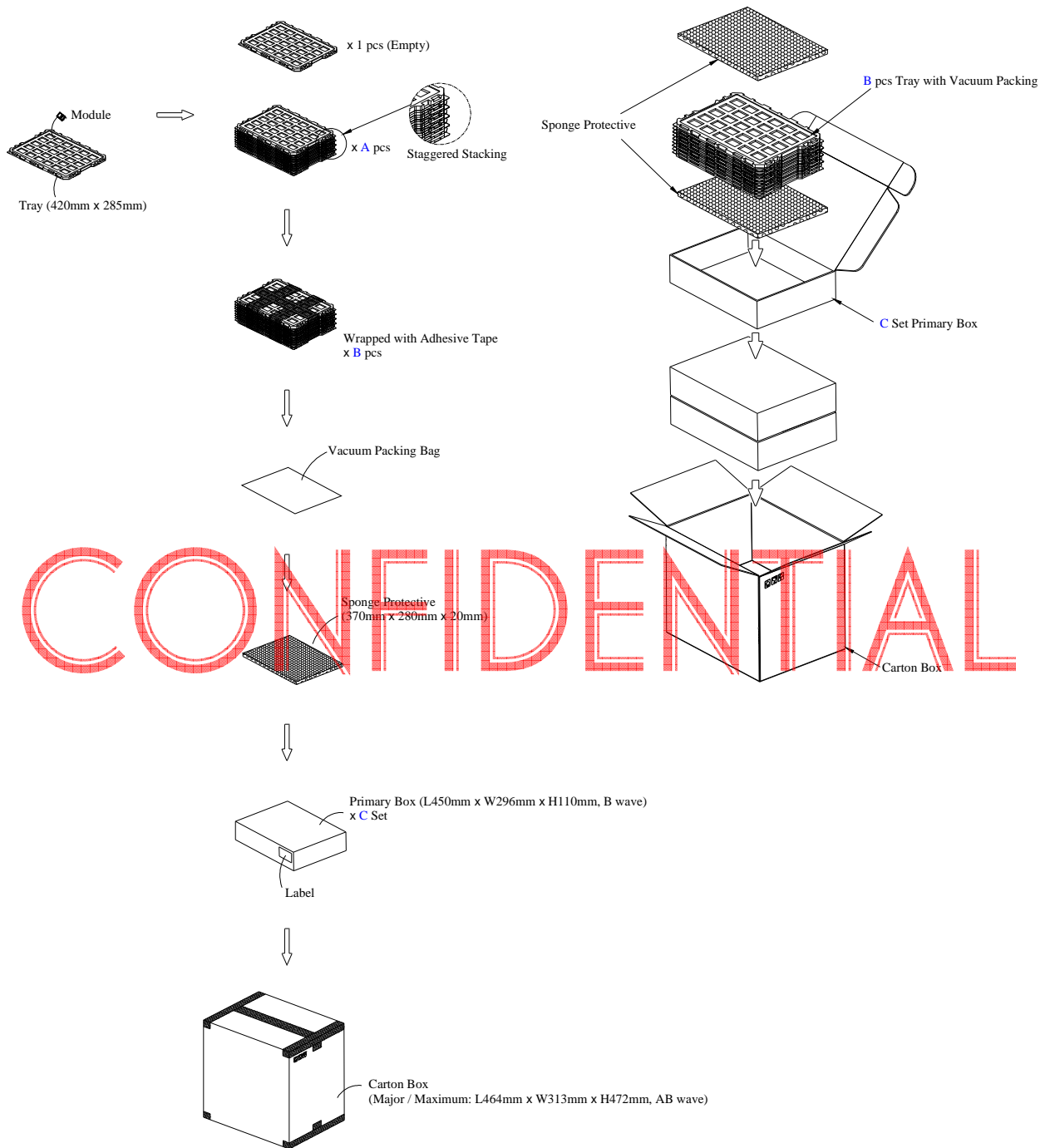
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6.3.3 Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major	

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7. Package Specifications

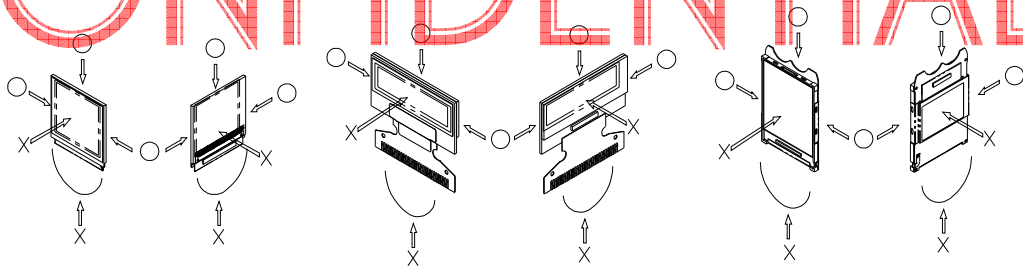


Item	Quantity	
Module	TBD	per Primary Box
Holding Trays (A)	TBD	per Primary Box
Total Trays (B)	TBD	per Primary Box (Including 1 Empty Tray)
Primary Box (C)	1~4	per Carton (4 as Major / Maximum)

8. Precautions When Using These OEL Display Modules

8.1 Handling Precautions

- 1) Since the display panel is being made of glass, do not apply mechanical impacts such as dropping from a high position.
- 2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
- 3) If pressure is applied to the display surface or its neighborhood of the OEL display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
- 4) The surface of the OEL display module is soft and easily scratched. Please be careful when handling the OEL display module.
- 5) When the surface of the OEL display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
 - * Scotch Mending Tape No. 810 or an equivalentNever try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol.
Also, pay attention that the following liquid and solvent may spoil the surface becoming cloudy without proper handling:
 - * Water
 - * Ketone
 - * Aromatic Solvents
- 6) Hold OEL display module very carefully when placing OEL display module into the system housing. Do not apply excessive stress or pressure to OEL display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.



- 7) Do not apply stress to the driver IC and the surrounding molded sections.
- 8) Do not disassemble nor modify the OEL display module.
- 9) Do not apply input signals while the logic power is off.
- 10) Pay sufficient attention to the working environments when handling OEL display modules to prevent occurrence of element breakage accidents by static electricity.
 - * Be sure to make human body grounding when handling OEL display modules.
 - * Be sure to ground tools to use or assembly such as soldering irons.
 - * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
 - * Protective film is being applied to the surface of the display panel of the OEL display module. Be careful since static electricity may be generated when exfoliating the protective film.
- 11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the OEL display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
- 12) If electric current is applied when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

8.2 Storage Precautions

- 1) When storing OEL display modules, put them in static electricity preventive bags avoiding exposure

to direct sun light nor to lights of fluorescent lamps. and, also, avoiding high temperature and high humidity environment or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from WiseChip Semiconductor Inc.)

At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.

- 2) If electric current is applied when water drops are adhering to the surface of the OEL display module, when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

8.3 Designing Precautions

- 1) The absolute maximum ratings are the ratings which cannot be exceeded for OEL display module, and if these values are exceeded, panel damage may be happen.
- 2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the V_{IL} and V_{IH} specifications and, at the same time, to make the signal line cable as short as possible.
- 3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (V_{DD}). (Recommend value: 0.5A)
- 4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
- 5) As for EMI, take necessary measures on the equipment side basically.
- 6) When fastening the OEL display module, fasten the external plastic housing section.
- 7) If power supply to the OEL display module is forcibly shut down by such errors as taking out the main battery while the OEL display panel is in operation, we cannot guarantee the quality of this OEL display module.
- 8) The electric potential to be connected to the rear face of the IC chip should be as follows: SH1107
* Connection (contact) to any other potential than the above may lead to rupture of the IC.

8.4 Precautions when disposing of the OEL display modules

- 1) Request the qualified companies to handle industrial wastes when disposing of the OEL display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

8.5 Other Precautions

- 1) When an OEL display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur. Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.
- 2) To protect OEL display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OEL display modules.
 - * Pins and electrodes
 - * Pattern layouts such as the FPC
- 3) With this OEL display module, the OEL driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OEL driver is exposed to light, malfunctioning may occur.
 - * Design the product and installation method so that the OEL driver may be shielded from light in actual usage.
 - * Design the product and installation method so that the OEL driver may be shielded from light during the inspection processes.
- 4) Although this OEL display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.

- 5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.

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Warranty:

The warranty period shall last twelve (12) months from the date of delivery. Buyer shall be completed to assemble all the processes within the effective twelve (12) months. WiseChip Semiconductor Inc. shall be liable for replacing any products which contain defective material or process which do not conform to the product specification, applicable drawings and specifications during the warranty period. All products must be preserved, handled and appearance to permit efficient handling during warranty period. The warranty coverage would be exclusive while the returned goods are out of the terms above.

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