# DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

SDLS119 – DECEMBER 1983 – REVISED MARCH 1988

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

## description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

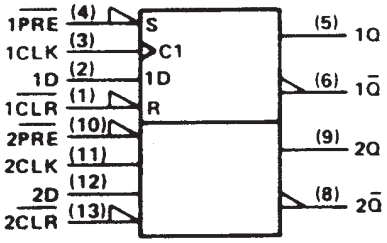
The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| $\overline{PRE}$ | $\overline{CLR}$ | CLK | D | Q | $\overline{Q}$ |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H† | H† |
| H | H | ↑ | H | H | L |
| H | H | ↑ | L | L | H |
| H | H | L | X | $Q_0$ | $\overline{Q}_0$ |

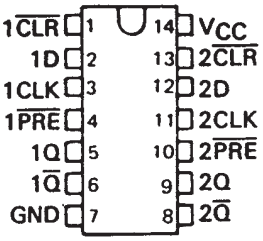
† The output levels in this configuration are not guaranteed to meet the minimum levels in $V_{OH}$ if the lows at preset and clear are near $V_{IL}$ maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

## logic symbol‡

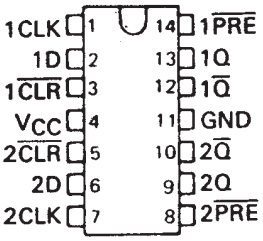



‡This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

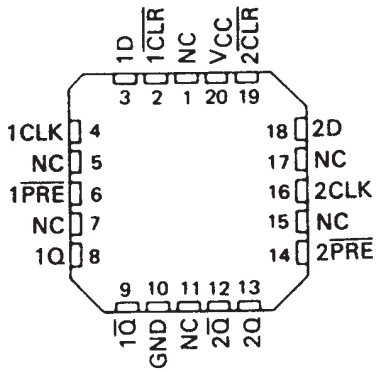
**SN5474 . . . J PACKAGE**
**SN54LS74A, SN54S74 . . . J OR W PACKAGE**
**SN7474 . . . N PACKAGE**
**SN74LS74A, SN74S74 . . . D OR N PACKAGE**
**(TOP VIEW)**




**SN5474 . . . W PACKAGE**
**(TOP VIEW)**

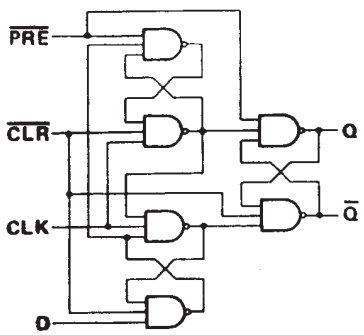



**SN54LS74A, SN54S74 . . . FK PACKAGE**
**(TOP VIEW)**




NC - No internal connection

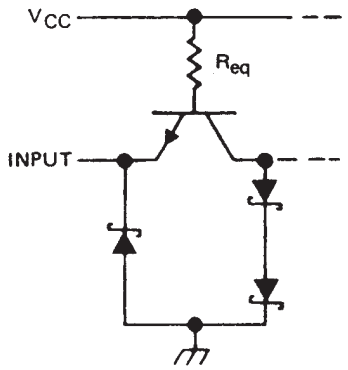
## logic diagram (positive logic)



## schematics of inputs and outputs

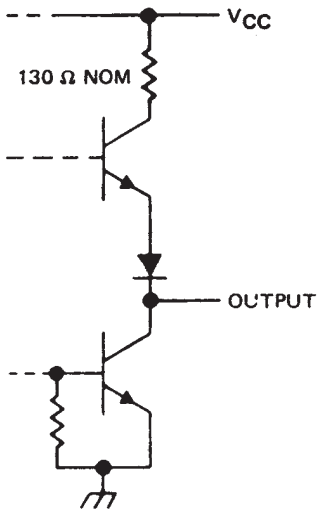
'74

EQUIVALENT OF EACH INPUT



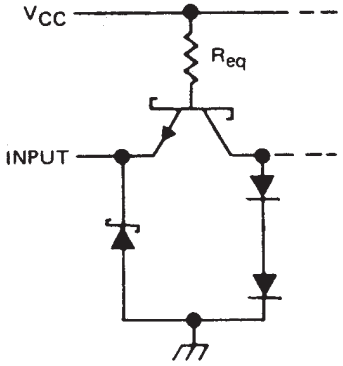

| $I_{IL}$ MAX | $R_{eq}$ NOM |
|---|---|
| –1.6 mA | 4 kΩ |
| –3.2 mA | 2 kΩ |

TYPICAL OF ALL OUTPUTS



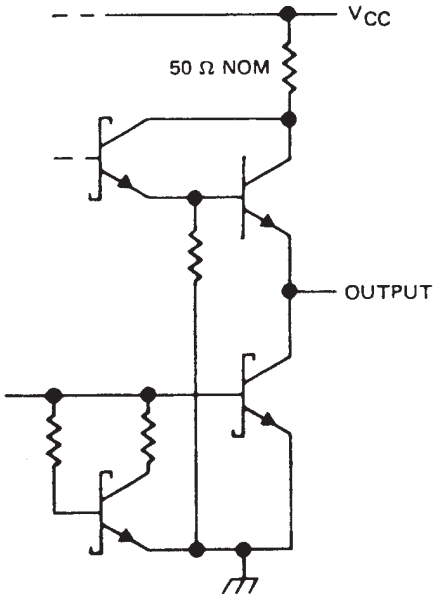

'S74

EQUIVALENT OF EACH INPUT



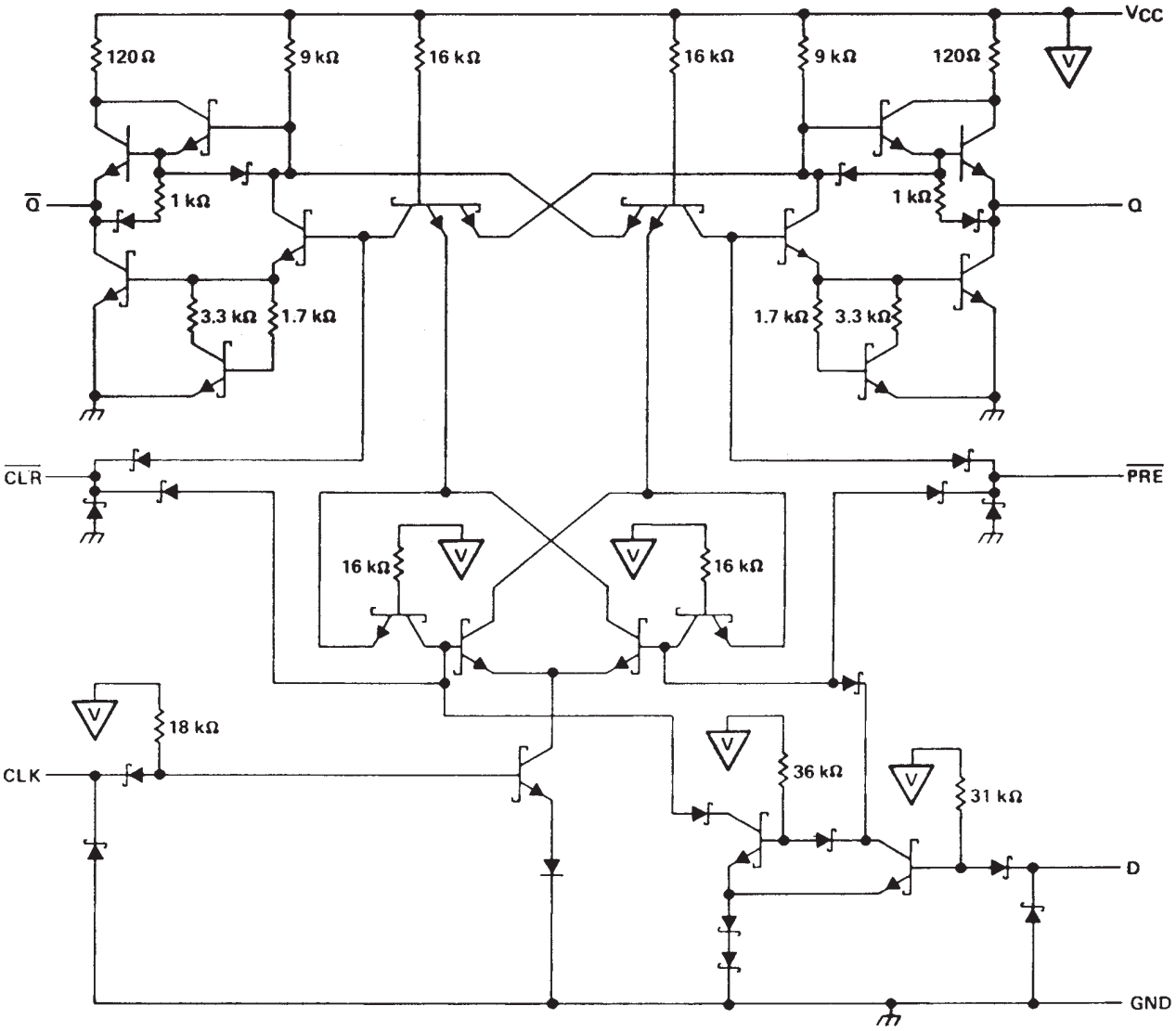

| $I_{IL}$ MAX | $R_{eq}$ NOM |
|---|---|
| –2 mA | 2.8 kΩ |
| –4 mA | 1.4 kΩ |
| –6 mA | 940 Ω |

TYPICAL OF ALL OUTPUTS



**schematic**

'LS74A




**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage: '74, 'S74 . . . . . 5.5 V
'LS74A . . . . . 7 V
Operating free-air temperature range: SN54' . . . . . −55°C to 125°C
SN74' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

| | | | SN5474 | | | SN7474 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | | −0.4 | | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | | | | 16 | | | 16 | mA |
| $t_w$ | Pulse duration | CLK high | 30 | | | 30 | | | ns |
| | | CLK low | 37 | | | 37 | | | |
| | | $\overline{PRE}$ or $\overline{CLR}$ low | 30 | | | 30 | | | |
| $t_{su}$ | Input setup time before CLK↑ | | 20 | | | 20 | | | ns |
| $t_h$ | Input hold time-data after CLK↑ | | 5 | | | 5 | | | ns |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | SN5474 | | | SN7474 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | | $V_{CC}$ = MIN, $I_I$ = −12 mA | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = −0.4 mA | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| $V_{OL}$ | | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 16 mA | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| $I_I$ | | $V_{CC}$ = MAX, $V_I$ = 5.5 V | | | 1 | | | 1 | mA |
| $I_{IH}$ | D | $V_{CC}$ = MAX, $V_I$ = 2.4 V | | | 40 | | | 40 | μA |
| | $\overline{CLR}$ | | | | 120 | | | 120 | |
| | All Other | | | | 80 | | | 80 | |
| $I_{IL}$ | D | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | | −1.6 | | | −1.6 | mA |
| | $\overline{PRE}$§ | | | | −1.6 | | | −1.6 | |
| | $\overline{CLR}$§ | | | | −3.2 | | | −3.2 | |
| | CLK | | | | −3.2 | | | −3.2 | |
| $I_{OS}$¶ | | $V_{CC}$ = MAX | −20 | | −57 | −18 | | −57 | mA |
| $I_{CC}$# | | $V_{CC}$ = MAX, See Note 2 | | 8.5 | 15 | | 8.5 | 15 | mA |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§Clear is tested with preset high and preset is tested with clear high.
¶Not more than one output should be shown at a time.
#Average per flip-flop.
NOTE 2: With all outputs open, $I_{CC}$ is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

## switching charateristics, $V_{CC}$ = 5 V, $T_A$ = 25°C (see note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{max}$ | | | $R_L$ = 400 Ω, $C_L$ = 15 pF | 15 | 25 | | MHz |
| $t_{PLH}$ | $\overline{PRE}$ or $\overline{CLR}$ | Q or $\overline{Q}$ | | | | 25 | ns |
| $t_{PHL}$ | | | | | | 40 | ns |
| $t_{PLH}$ | CLK | Q or $\overline{Q}$ | | | 14 | 25 | ns |
| $t_{PHL}$ | | | | | 20 | 40 | ns |

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

## recommended operating conditions

| | | | SN54LS74A | | | SN74LS74A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.7 | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | | −0.4 | | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | | | | 4 | | | 8 | mA |
| $f_{clock}$ | Clock frequency | | 0 | | 25 | 0 | | 25 | MHz |
| $t_w$ | Pulse duration | CLK high | 25 | | | 25 | | | ns |
| | | $\overline{PRE}$ or $\overline{CLR}$ low | 25 | | | 25 | | | |
| $t_{su}$ | Setup time-before CLK↑ | High-level data | 20 | | | 20 | | | ns |
| | | Low-level data | 20 | | | 20 | | | |
| $t_h$ | Hold time-data after CLK↑ | | 5 | | | 5 | | | ns |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | | SN54LS74A | | | SN74LS74A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | | $V_{CC}$ = MIN, | $I_I$ = −18 mA | | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | | $V_{CC}$ = MIN, $I_{OH}$ = −0.4 mA | $V_{IH}$ = 2 V, | $V_{IL}$ = MAX, | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| $V_{OL}$ | | $V_{CC}$ = MIN, $I_{OL}$ = 4 mA | $V_{IL}$ = MAX, | $V_{IH}$ = 2 V, | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | $V_{CC}$ = MIN, $I_{OL}$ = 8 mA | $V_{IL}$ = MAX, | $V_{IH}$ = 2 V, | | | | | 0.35 | 0.5 | |
| $I_I$ | D or CLK | $V_{CC}$ = MAX, | $V_I$ = 7 V | | | | 0.1 | | | 0.1 | mA |
| | $\overline{CLR}$ or $\overline{PRE}$ | | | | | | 0.2 | | | 0.2 | |
| $I_{IH}$ | D or CLK | $V_{CC}$ = MAX, | $V_I$ = 2.7 V | | | | 20 | | | 20 | μA |
| | $\overline{CLR}$ or $\overline{PRE}$ | | | | | | 40 | | | 40 | |
| $I_{IL}$ | D or CLK | $V_{CC}$ = MAX, | $V_I$ = 0.4 V | | | | −0.4 | | | −0.4 | mA |
| | $\overline{CLR}$ or $\overline{PRE}$ | | | | | | −0.8 | | | −0.8 | |
| $I_{OS}$§ | | $V_{CC}$ = MAX, | See Note 4 | | −20 | | −100 | −20 | | −100 | mA |
| $I_{CC}$ (Total) | | $V_{CC}$ = MAX, | See Note 2 | | | 4 | 8 | | 4 | 8 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: With all outputs open, $I_{CC}$ is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.
NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with $V_O$ = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C (see note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | | | $R_L$ = 2 kΩ, | $C_L$ = 15 pF | 25 | 33 | | MHz |
| $t_{PLH}$ | $\overline{CLR}$, $\overline{PRE}$ or CLK | Q or $\overline{Q}$ | | | | 13 | 25 | ns |
| $t_{PHL}$ | | | | | | 25 | 40 | ns |

Note 3: Load circuits and voltage waveforms are shown in Section 1.

## recommended operating conditions

| | | | SN54S74 | | | SN74S74 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | | −1 | | | −1 | mA |
| $I_{OL}$ | Low-level output current | | | | 20 | | | 20 | mA |
| $t_w$ | Pulse duration | CLK high | 6 | | | 6 | | | ns |
| | | CLK low | 7.3 | | | 7.3 | | | |
| | | $\overline{CLR}$ or $\overline{PRE}$ low | 7 | | | 7 | | | |
| $t_{su}$ | Setup time, before CLK ↑ | High-level data | 3 | | | 3 | | | ns |
| | | Low-level data | 3 | | | 3 | | | |
| $t_h$ | Input hold time - data after CLK ↑ | | 2 | | | 2 | | | ns |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | SN54S74 | | | SN74S74 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | | $V_{CC}$ = MIN, $I_I$ = −18 mA, | | | −1.2 | | | −1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = −1 mA | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| $V_{OL}$ | | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 20 mA | | | 0.5 | | | 0.5 | V |
| $I_I$ | | $V_{CC}$ = MAX, $V_I$ = 5.5 V | | | 1 | | | 1 | mA |
| $I_{IH}$ | D | $V_{CC}$ = MAX, $V_I$ = 2.7 V | | | 50 | | | 50 | μA |
| | $\overline{CLR}$ | | | | 150 | | | 150 | |
| | $\overline{PRE}$ or CLK | | | | 100 | | | 100 | |
| $I_{IL}$ | D | $V_{CC}$ = MAX, $V_I$ = 0.5 V | | | −2 | | | −2 | mA |
| | $\overline{CLR}$¶ | | | | −6 | | | −6 | |
| | $\overline{PRE}$¶ | | | | −4 | | | −4 | |
| | CLK | | | | −4 | | | −4 | |
| $I_{OS}$§ | | $V_{CC}$ = MAX | −40 | | −100 | −40 | | −100 | mA |
| $I_{CC}$# | | $V_{CC}$ = MAX, See Note 2 | | 15 | 25 | | 15 | 25 | mA |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
¶Clear is tested with preset high and preset is tested with clear high.
#Average per flip-flop.
NOTE 2: With all outputs open, $I_{CC}$ is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C (see note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{max}$ | | | $R_L$ = 280 Ω, $C_L$ = 15 pF | 75 | 110 | | MHz |
| $t_{PLH}$ | $\overline{PRE}$ or $\overline{CLR}$ | Q or $\overline{Q}$ | | | 4 | 6 | ns |
| $t_{PHL}$ | $\overline{PRE}$ or $\overline{CLR}$ (CLK high) | $\overline{Q}$ or Q | | | 9 | 13.5 | ns |
| | $\overline{PRE}$ or $\overline{CLR}$ (CLK low) | | | | 5 | 8 | |
| $t_{PLH}$ | CLK | Q or $\overline{Q}$ | | | 6 | 9 | ns |
| $t_{PHL}$ | | | | | 6 | 9 | ns |

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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