

74AC273 • 74ACT273 Octal D-Type Flip-Flop

General Description

The AC273 and ACT273 have eight edge-triggered D-type flip-flops with individual D-type inputs and Q outputs. The common buffered Clock (CP) and Master Reset (MR) input load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D-type input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the MR input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

Features

- Ideal buffer for microprocessor or memory
- Eight edge-triggered D-type flip-flops
- Buffered common clock
- Buffered, asynchronous master reset
- See 377 for clock enable version
- See 373 for transparent latch version
- See 374 for 3-STATE version
- Outputs source/sink 24 mA
- 74ACT273 has TTL-compatible inputs

Ordering Code:

Order Number	Package Number	Package Description
74AC273SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74AC273SJ	M20D	Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC273MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC273PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT273SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ACT273SJ	M20D	Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT273MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT273MTCX_NL (Note 1)	MTC20	Pb-Free 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT273PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

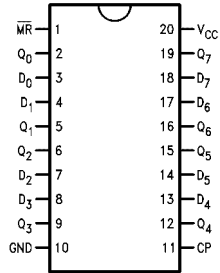
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

Note 1: "_NL" indicates Pb-Free package (per JEDEC J-STD-020B). Device available in Tape and Reel only.

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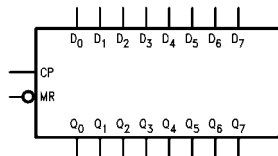
Connection Diagram



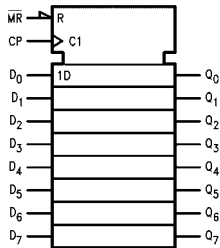
Pin Descriptions

Pin Names	Description
D ₀ -D ₇	Data Inputs
MR	Master Reset
CP	Clock Pulse Input
Q ₀ -Q ₇	Data Outputs

Logic Symbols



IEEE/IEC

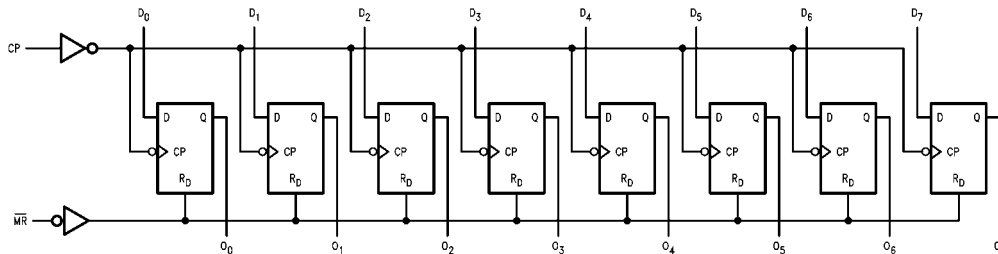


Mode Select-Function Table

Operating Mode	Inputs			Outputs
	MR	CP	D _n	Q _n
Reset (Clear)	L	X	X	L
Load '1'	H	↗	H	H
Load '0'	H	↘	L	L

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 ↗ = LOW-to-HIGH Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 2)

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	± 50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	± 50 mA
Storage Temperature (T_{STG})	-65°C to +150°C
Junction Temperature (T_J) (PDIP)	140°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
AC	2.0V to 6.0V
ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	-40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V for AC	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V for ACT	125 mV/ns

Note 2: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, with-out exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V)	$T_A = +25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	Units	Conditions	
			Typ	Guaranteed Limits				
V_{IH}	Minimum HIGH Level Input Voltage	3.0	1.5	2.1	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V_{IL}	Maximum LOW Level Input Voltage	3.0	1.5	0.9	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V_{OH}	Minimum HIGH Level Output Voltage	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50 \mu\text{A}$	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
			3.0		2.56	2.46	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -12 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA (Note 3)}$
			4.5		3.86	3.76		
			5.5		4.86	4.76		
V_{OL}	Maximum LOW Level Output Voltage	3.0	0.002	0.1	0.1	V	$I_{OUT} = 50 \mu\text{A}$	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
			3.0		0.36	0.44	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA (Note 3)}$
			4.5		0.36	0.44		
			5.5		0.36	0.44		
I_{IN} (Note 5)	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	μA	$V_I = V_{CC}, \text{ GND}$	
I_{OLD}	Minimum Dynamic	5.5			75	mA	$V_{OLD} = 1.65V \text{ Max}$	
I_{OHD}	Output Current (Note 4)	5.5			-75	mA	$V_{OHD} = 3.85V \text{ Min}$	
I_{CC} (Note 5)	Maximum Quiescent Supply Current	5.5		4.0	40.0	μA	$V_{IN} = V_{CC}$ or GND	

Note 3: All outputs loaded; thresholds on input associated with output under test.

Note 4: Maximum test duration 2.0 ms, one output loaded at a time.

Note 5: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} .

AC Electrical Characteristics for AC

Symbol	Parameter	V _{CC} (V) (Note 6)	T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF		Units
			Min	Typ	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	3.3	90	125		75	MHz	
		5.0	140	175		125		
t _{PLH}	Propagation Delay Clock to Output	3.3	4.0	7.0	12.5	3.0	14.0	ns
		5.0	3.0	5.5	9.0	2.5	10.0	
t _{PHL}	Propagation Delay Clock to Output	3.3	4.0	7.0	13.0	3.5	14.5	ns
		5.0	3.0	5.0	10.0	2.5	11.0	
t _{PHL}	Propagation Delay \overline{MR} to Output	3.3	4.0	7.0	13.0	3.5	14.0	ns
		5.0	3.0	5.0	10.0	2.5	10.5	

Note 6: Voltage Range 3.3 is 3.3V ± 0.3V

Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements for AC

Symbol	Parameter	V _{CC} (V) (Note 7)	T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		Units
			Typ	Guaranteed Minimum			
t _S	Setup Time, HIGH or LOW Data to CP	3.3	3.5	5.5	6.0		ns
		5.0	2.5	4.0	4.5		
t _H	Hold Time, HIGH or LOW Data to CP	3.3	-2.0	0	0		ns
		5.0	-1.0	1.0	1.0		
t _W	Clock Pulse Width HIGH or LOW	3.3	3.5	5.5	6.0		ns
		5.0	2.5	4.0	4.5		
t _W	\overline{MR} Pulse Width HIGH or LOW	3.3	2.0	5.5	6.0		ns
		5.0	1.5	4.0	4.5		
t _{rec}	Recovery Time \overline{MR} to CP	3.3	1.5	3.5	4.5		ns
		5.0	1.0	2.0	3.0		

Note 7: Voltage Range 3.3 is 3.3V ± 0.3V

Voltage Range 5.0 is 5.0V ± 0.5V

DC Electrical Characteristics for ACT

Symbol	Parameter	V _{CC} (V)	T _A = +25°C		T _A = -40°C to +85°C		Units	Conditions
			Typ	Guaranteed Limits				
V _{IH}	Minimum HIGH Level Input Voltage	4.5	1.5	2.0		2.0	V	V _{OUT} = 0.1V or V _{CC} - 0.1V
		5.5	1.5	2.0		2.0		
V _{IL}	Maximum LOW Level Input Voltage	4.5	1.5	0.8		0.8	V	V _{OUT} = 0.1V or V _{CC} - 0.1V
		5.5	1.5	0.8		0.8		
V _{OH}	Minimum HIGH Level Output Voltage	4.5	4.49	4.4		4.4	V	I _{OUT} = -50 μA
		5.5	5.49	5.4		5.4		
		4.5		3.86		3.76		
V _{OL}	Maximum LOW Level Output Voltage	4.5	0.001	0.1		0.1	V	I _{OH} = -24 mA I _{OH} = -24 mA (Note 8)
		5.5	0.001	0.1		0.1		
		4.5		0.36		0.44		
V _{OL}	Maximum LOW Level Output Voltage	5.5		0.36		0.44	V	V _{IN} = V _{IL} or V _{IH} I _{OL} = 24 mA I _{OL} = 24 mA (Note 8)
		4.5		0.36		0.44		
I _{IN}	Maximum Input Leakage Current	5.5		±0.1		±1.0	μA	V _I = V _{CC} , GND
I _{CC}	Maximum I _{CC} /Input	5.5	0.6		1.5		mA	V _I = V _{CC} - 2.1V
I _{OLD}	Minimum Dynamic Output Current (Note 9)	5.5				75	mA	V _{OLD} = 1.65V Max
I _{OHD}	Maximum Dynamic Output Current (Note 9)	5.5				-75	mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0		40.0	μA	V _{IN} = V _{CC} or GND

Note 8: All outputs loaded; thresholds on input associated with output under test.

Note 9: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics for ACT

Symbol	Parameter	V _{CC} (V) (Note 10)	T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF		Units
			Min	Typ	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	2.0	125	189		110		MHz
t _{PLH}	Propagation Delay CP to Q _n	5.0	1.5	6.5	8.5	1.5	9.0	ns
t _{PHL}	Propagation Delay MR to Q _n	5.0	1.5	7.0	9.0	1.5	8.5	ns

Note 10: Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements for ACT

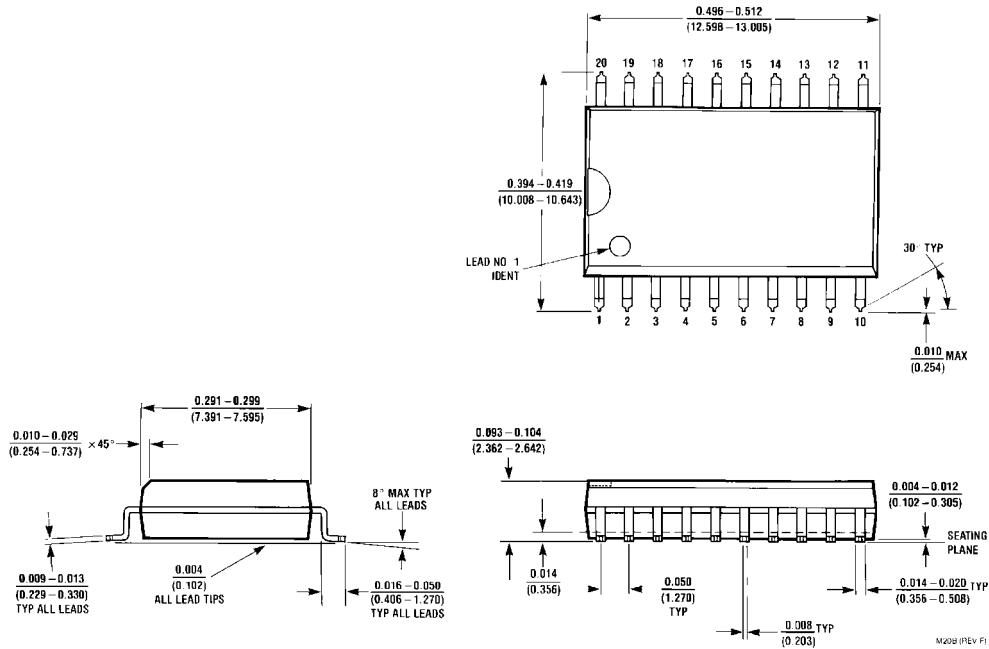
Symbol	Parameter	V _{CC} (V) (Note 11)	T _A = +25°C		T _A = -40°C to +85°C		Units
			C _L = 50 pF		C _L = 50 pF		
			Typ	Guaranteed Minimum			
t _S	Setup Time, HIGH or LOW D _n to CP	5.0	1.0	3.5	3.5	ns	
t _H	Hold Time, HIGH or LOW D _n to CP	5.0	-0.5	1.5	1.5	ns	
t _W	Clock Pulse Width HIGH or LOW	5.0	2.0	4.0	4.0	ns	
t _W	$\overline{\text{MR}}$ Pulse Width HIGH or LOW	5.0	1.5	4.0	4.0	ns	
t _W	Recovery Time $\overline{\text{MR}}$ to CP	5.0	0.5	3.0	3.0	ns	

Note 11: Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

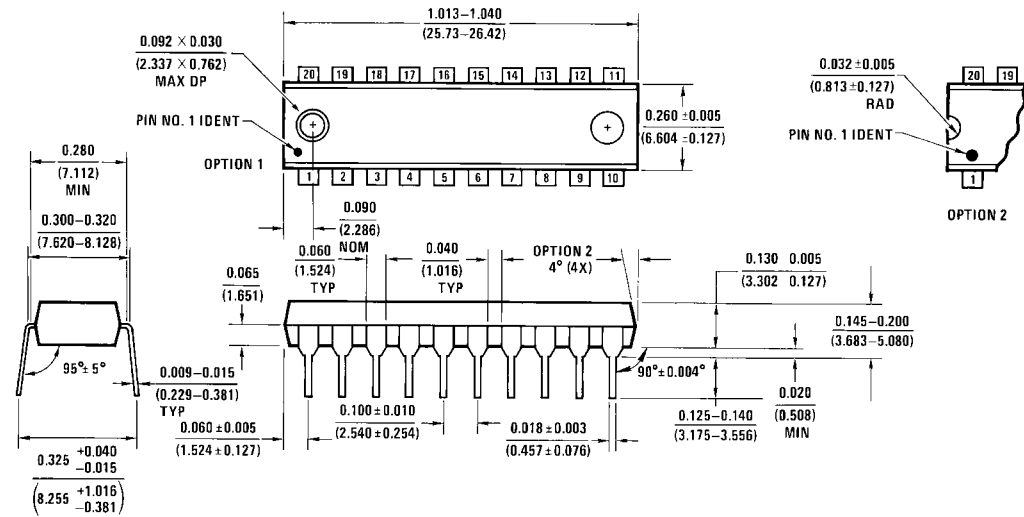
Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN
C _{PD}	Power Dissipation Capacitance for AC Power Dissipation Capacitance for ACT	50.0 40.0	pF	V _{CC} = 5.0V

Physical Dimensions inches (millimeters) unless otherwise noted



**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



N20A (REV G)

**20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A**

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